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FUNDAMENTAL INVESTIGATION OF DIGITAL COMPUTER STORAGE AND ACCESS TECHNIQUES

S. W. Miller

Stanford Research Institute
Menlo Park, California

SRI Project 3184

Contract AF30(602)-2227

Prepared
for

Rome Air Development Center
Air Force Systems Command
United States Air Force

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FOREWORD

This report, and the Technical Supplement (RADC-TR-61-117B) bound separately and entitled "Magnetic Core Access Switches," were prepared by the Computer Techniques Laboratory of Stanford Research Institute, Menlo Park, California, on Contract AF 30(602)-2227 with RADC. The research work covered the period from 1 April 1960 to 1 April 1961; this report and the Technical Supplement are the final reports on this work.

The contract efforts were performed under the cognizance of the Information Processing Laboratory, Data Processing Branch (RAWID), Rome Air Development Center with Mr. Senatro J. Iuorno as Project Engineer.

ABSTRACT

We have used the artifice of a conceptual model of a storage unit in order to classify the various kinds of storage units according to their terminal characteristics. The important terminal characteristics are the storage capacity, speed and order of access, the operating mode, and the permanence of the stored data. We dissected this model into four fundamental parts, an aggregate of storage registers, access equipment for selection and excitation of the desired register, the sensing equipment for determining the data stored in the register, and the organizational scheme used for their interconnection. The various techniques for achieving these fundamental operations, either in use or being developed, are outlined and discussed. The relation between the use of particular techniques in a storage unit and the position of that storage unit on the capacity *vs* speed graph is shown with some predictions for improvements.

ACKNOWLEDGEMENT

The author wishes gratefully to acknowledge the origination and guidance of this project by Mr. J. Reid Anderson, Manager, Computer Techniques Laboratory, the help and criticism of the material presented by Dr. Robert C. Minnick, the compilation of material on sensing by Mr. Leroy Younker, the very excellent research work on magnetic core access switches (Technical Supplement) by Mr. John L. Haynes and Dr. Minnick, and the work in gathering bibliographic material by Mr. W. W. Stevens.

ABSTRACT
OF TECHNICAL SUPPLEMENT

A number of the more commonly known magnetic core access switches are combined in a single analytical model. In addition to yielding as special cases the known access switches on which it is based, this model produces many apparently new switches. Relationships among the various parameters in this model are developed in such a way that the designer may choose the number of drivers, the load-sharing factor, the number of turns of wire per switch core and the magnitude of the maximum disturbing magnetomotive force within certain limits. As further aids to the designer, a number of tables are included and algorithms are given which may be used to match the switch properties closely to the design requirements. Several methods are developed for economizing on the number of drivers used in switches, and certain special access switches are treated. The current knowledge is reviewed on a fairly recent and important class of access switches, known as load-sharing zero-noise switches. These switches are compared with one another, and a fundamental theorem is proved that such switches can have no more outputs than inputs. Several new classes of load-sharing zero-noise switches are developed and analyzed; in particular, switches are developed which for a given number of outputs allow more flexibility in the choice of the load-sharing factor than formerly was the case.

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FUNDAMENTAL INVESTIGATION OF DIGITAL STORAGE AND ACCESS TECHNIQUES

I INTRODUCTION

The purpose of this report was to re-examine, classify, and study existing and new storage and access techniques. The aim of such a study is to gain a better understanding of the fundamental principles of storage and access techniques so that better selections can be made of the promising new research and development areas to pursue in this field. The work is presented in two parts. The first is a broad survey and classification of storage units and their fundamental parts. The second part, under separate cover and titled "*Magnetic Core Access Switches, Technical Supplement to RADC-TR-61-117A,*" covers a detailed study of the very crucial area of access to stored data. Very early in the survey part of the project, it was found that access techniques had received considerably less attention in the literature than had storage. As storage capacity of new units increases, a greater burden is placed on design techniques for access. The abstract of that study report appears on page ix of this volume.

The survey portion of the work is presented in four sections; each section contains many bibliographic references for further details on particular techniques.

Section II presents a conceptual model of a digital storage system. Through this model we are able to define a digital storage system as any system having a set of three distinct types of inputs, entitled *data*, *address*, and *control* and a single *data output* which is displaced in time. We next classify existing and possible types of storage units into different functional groups or classes, according to the characteristics observable at these terminals.

II CLASSIFICATION ACCORDING TO TERMINAL CHARACTERISTICS

A. GENERAL DEFINITIONS

The definition of elementary concepts and the terminology used throughout the report are stated here for clarity.

Digital computers are classically composed of five basic units: (1) input, (2) storage, (3) arithmetic, (4) switching and control, and (5) output. This investigation is concerned with equipment and techniques used primarily in storage units. The sum of remaining units will be referred to in this report as the "parent system." The terminals of a storage unit, then, are its connections with the parent system. The functions of the storage unit are: (1) to receive digital data and control information via these terminals, (2) retain this data inviolate until some later time and (3) return it to the parent system upon request. A great deal can be said about how these functions are performed from the characteristics at the terminals alone, without knowing the additional details of the circuits and techniques employed internal to the storage unit.

In order to facilitate such discussions we will introduce the simple conceptual model of a storage unit shown in Fig. 1. This model is shown with four sets of terminals (separate from any power inputs): (1) address, (2) control, (3) data input and (4) data output. Since we are concerned here only with digital storage units, the types of signals carried by these terminals are, of necessity, digital. As such, a terminal may be a single pair of leads carrying serial data, or many leads carrying data

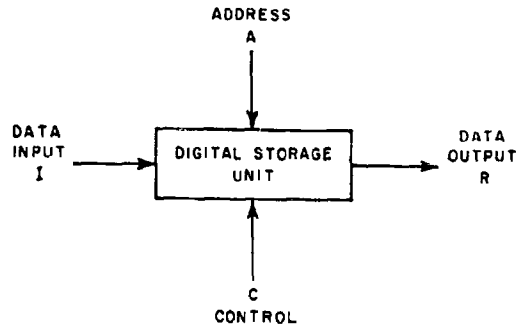


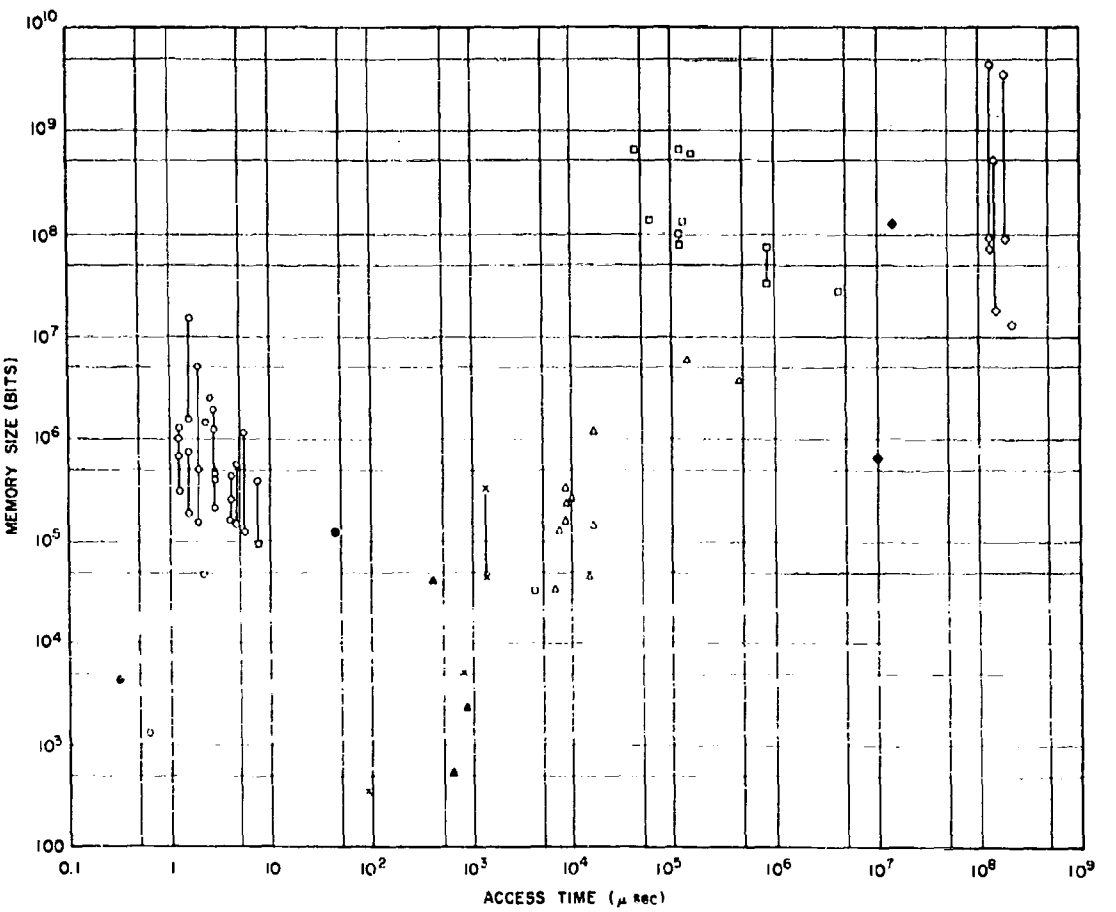
FIG. 1
CONCEPTUAL MODEL OF A STORAGE UNIT
(This shows only the terminals)

in parallel. Also, the digital data may be represented by voltage pulses or levels, current pulses or levels or whatever scheme is used by the parent system and are assumed to enter our model storage unit via a "register" which converts the inputs to whatever logic form required by the storage unit and which reconverts the outputs to match the parent system.

The data inputs and data outputs of our conceptual model will be in words of a fixed number of bits. The number of bits in this word is determined in the design of the parent system and governs the number of leads in either the data input or output terminals. Of course, if the data are bit serial, the word size controls only the time required to enter or leave the model. Each of these words is associated with a particular address—that is, upon inserting data into the storage unit, the parent system assigns an address to each word it wishes to store. For the parent system to retrieve a word, it must repeat the address to which that word was assigned. The *storage capacity* of a storage unit can thus be reckoned in two ways, either by the number of available addresses for word storage or, more commonly, by this number of words multiplied by the number of bits per word. This latter is referred to as *bit capacity*.

The time elapsed from the point when the parent system requests a stored word until that word is made available to the parent system by the storage unit is called the *read access time*. The time during which the parent system must wait between two requests for data from the storage unit is called the *read cycle time*. Likewise, the time elapsed between the storage of two words in different addresses is called the *write cycle time*. Variations of these terms appropriate to individual types of storage units will be introduced with the particular type.

In Fig. 2 is shown a graph of the logarithm of bit capacity versus the logarithm of average read access time for a number of typical storage units. The read access time is used in preference to read/write cycle time in order to more accurately compare with read-only storage units. When read access time could not be quoted separately from R/W cycle time, half of the value of the latter was used. The average of variable read access times was used for simplicity. The logarithm of these quantities was used primarily for range compression; however its use clearly shows a division of available units into two groups, one of closely packed points on the left and the other more loosely spread on the right. The existence



LEGEND:

- ○ MAGNETIC CORES
- ◆ MAGNETIC THIN FILM
- △ MAGNETIC DRUM
- ▲ MAGNETIC DRUM HIGH SPEED REGISTER
- ■ PHOTOGRAPHIC
- □ MAGNETIC DISC
- ○ MAGNETIC TAPE
- ◆ MAGNETIC TAPE STRIPS
- × MAGNETOSTRICTIVE DELAY LINE
- • MODULATED COUPLING

FIG. 2

CAPACITY VS. SPEED GRAPH
(For storage units in representative digital systems in operation in 1961)

of these two groups has been recognized by many, and they have received a variety of names, such as primary and secondary units, electronic and mechanical storage units, working and back-up storage units, and high- and low-speed storage units. None of these dichotomies fits exactly the descriptions that follow and we shall prefer to call them high-speed and back-up groups of storage units. A third group exists (*not* represented in Fig. 2) in which the capacity is effectively unlimited. Examples of storage units in this third group are magnetic tape, punched paper tape and punched card units where blocks of the storage medium may be manually removed and stored in a warehouse. Such storage units are very similar to input/output units and occasionally are referred to as *external storage units* as opposed to the internal storage units of Fig. 2. The use of several storage units of increasing capacity and increasing read-access time in the same computing system is called a hierarchy of storage units. Such hierarchies exist because back-up storage units can provide large capacity storage at a considerably smaller cost per bit than can high-speed stores.

B. CLASSIFICATION

Two terminal characteristics (capacity and speed) have already been mentioned. Three others which provide the basis for classifying kinds of storage units are (1) the operating mode, (2) the order of access and (3) the permanence of the stored data.

1. Operating Mode

The *addressable mode* is the most common operating mode of storage units and was the mode assumed for the operations discussed in Part A.

There are two independent phases to the operation, (1) that of inserting or storing data in the storage unit, and (2) that of retrieving data from it. The former we will call the *write phase* and the latter the *read phase*.

For the operation of the write phase the storage unit must have three sets of signals from the parent system. It must have the word to be stored or data input, the address in which it is to be stored and a control signal indicating the desire and time to store data. In the conceptual model of Fig. 1, these are shown with arrowheads indicating

inputs. The data and address inputs must either be available from the parent system at the moment the control signal indicates the start of a write phase, or they must be available just prior to the control signal and held in registers within the storage unit until used.

In order to retrieve a word previously stored, it is necessary for the parent system to supply two sets of inputs: (1) the address at which the desired word is stored, and (2) the control signal to read. In this case whatever data had been previously written into the storage register of this location will appear as a data output.

Specifically these two phases may be described by the relation

$$W(t) = f[A(t),\ I(t),\ C_W(t)]$$

$$R(t + \Delta t) = f[A(t + \Delta t),\ C_R(t + \Delta t),\ W(t)]$$

if

$$A(t + \Delta t) = A(t) \quad .$$

Here, W and R stand for the two phases, write and read respectively, t indicates the time of C_W or the initiation by control of the write phase, $t + \Delta t$ indicates the time of C_R or the initiation of the read phase, and and A and I are the address and data or information inputs. W and R essentially mean "the proper functioning of" their particular phase, hence R requires an output while W does not.

A second important operating mode is the *content addressed mode.* As before, this is a two-phase mode--indeed, the write phase is identical in both modes. The difference is in the read phase, where all or a portion of the stored digital data is made part of the input of this read phase rather than the address. Output can be derived in several forms. The most familiar operation is a search for stored data on the basis of a known word or partial word. Here the word (or portion of it) is presented as an input and compared with all stored words serially until a match is found. In this case the output will be the remainder of the stored word or a unit record of a given number of stored words following the input data word. This is possible in many magnetic drum and tape

storage units. (This is distinct from the ability of a parent system to give an addressable storage unit successive addresses until the searched for data word comes out; here, the storage unit must recognize the match between input and output data.)

Recent storage units have been described[1] which permit the quizzing of all storage registers in parallel for a match with the data input. Such storage units are given the name of "associative" units to differentiate this type of content addressing from the serial scanning mentioned above. Associative storage units may be *fully associative*, and the entire stored data word used as input. In this case the output may be either the *address* at which it was stored, or simply *yes* or *no*, according to whether the input word is or is not contained within the storage unit. A *partially associative mode* refers to a storage unit which is capable of accepting a variable-length field which is a fractional part of the full data word stored.[2]

The *tag mode* is an associative mode in which the storage unit accepts a fixed portion of the stored data word as an input. The *partial tag mode* may accept a variable fraction of this tag, as follows:

$$R(t + \Delta t) = f[I(t + \Delta t),\ W(t)]$$

$$I(t + \Delta t) = I(t)$$

or some field of $I(t)$.

The third operating mode of importance is the *buffer mode*. Buffer storage units also operate in a write and read phase. During the write phase, only the data word and control signal are presented as inputs, and no address is specified. During the read phase, only the control signal is an input and the data words are read out in the order in which they were stored, *i.e.*, "first in, first out." Such storage units are generally used to couple slow input/output units to higher-speed parent systems. They are not considered as internal storage; however, the components and techniques are essentially the same as those of the other units considered. Recently a "pushdown buffer" has been announced[3] for use as a special-purpose internal storage unit. This type of buffer differs only in that it is "last in, first out."

A large class of growing importance is that of the fixed or permanent storage units. These do not have a write phase, as such, since the stored

data were essentially wired in when the unit was built. This permits a wide variety of new techniques to be used. Such units are used for table look-up, program storage, or sub-routine storage. Closely related is the semi-permanent or slow-write, fast-read storage units in which the data are more readily changeable.

It should be pointed out that the List[4] and Trie[5] memories are not operating modes of hardware storage units *per se*, rather they are ways in which an addressable, erasable, random access storage unit may be reconfigured by a programmer to make it particularly useful for the solution of certain classes of problems.

2. Order of Access

Another very useful way of classifying storage units according to their terminals is by *Order of Access*, which refers to the way in which successive input addresses are interrelated.

If the presentation of a particular address to the storage unit as an input is completely independent of the past history of addresses presented to the unit, then the order of access is said to be *random access*. That is, from the terminals one can at any time address any particular storage register with essentially equal elapsed time without affecting the time required to retrieve data from the next address given. This random order of access implies the input address is decoded to a selected storage register which is then coupled to the information input in such a fashion that there is nothing unique about any particular order of addressing these registers.

Today, virtually all high-speed, random-access storage units in general-purpose computers use storage registers of magnetic cores.

The *Order of Access* is said to be *cyclic access* if the addresses are arranged serially, must be traversed in one direction, and if the first address follows immediately after the last address. Such is the case, for instance, with a magnetic drum. The read access time for any particular address is thus history dependent, *i.e.*, it depends upon the number of addresses between the one coupled to the input at the instant the input signals are available and the desired address. For example, if a particular system is coupled to Address 1, has 10 addresses in a track,

and desires to couple to Address m, then the time to cycle through 1, 2, 3, ..., m must elapse. On the other hand, if at the instant the input signals indicated a desire to couple to m, the equipment was coupled to m - 1 then a minimum time would be required for read access. Again, to move from m + 1 to m requires traversing the entire track of m addresses and hence a maximum read access time. It is seen from this discussion that *read access time* actually has no meaning in a cyclic order of access; instead, the *average read access time* should be used, which is defined as 1/2 (min + max access times). Of course occasionally one can beat the average time by being clever.

• Cyclic access is achieved primarily by the use of rotating equipment such as magnetic drums and disc. The use of delay lines also produces cyclic access.

If the addresses are arranged in an essentially linear fashion (as in a reel of magnetic tape), so that to progress serially from any address to any other requires passing all intervening addresses, the order is *serial access*. Such schemes are usually reversible, *i.e.*, they can be moved from higher-numbered addresses to lower and vice versa with equal ease. Thus it is seen that the elapsed time in getting from one address to another is dependent on the *number* of intervening addresses but not on the direction. The time from highest numbered address to the lowest is a maximum rather than a minimum, and is the same as the time required to progress from the lowest numbered address to the highest. Hence, the average read-access time as defined for cyclic access is important when the storage unit is given single address inputs at random. There is an additional parameter which is used if a large block of addresses are to be requested simultaneously. This is the rate of data transfer; it involves the elapsed time in moving from one address to the adjacent address and the amount of data obtained from that address.

Serial access is most often found in magnetic or punched paper tapes, punched cards and similar storage units. These have much in common with input/output units and often are distinguished from them only by the manner in which tapes and cards are used.

The order of access is the principal determinant of the amount of time consumed in the execution of a particular type of problem on the computer. Random order generally takes the least elapsed time but requires the most

equipment (and therefore expense). Serial order requires the least access equipment for a given storage capacity but takes the most elapsed time. Many studies[6,7] have been made to determine how much equipment expense is justified to save time. Each depends on the particular problem, its urgency and available funds.

3. Permanence of the Stored Data

The third major way of classifying memory systems according to effects observable from the terminals is by the permanence of the stored data. This permanence is controlled directly by the components, media, or techniques used to construct the storage registers themselves, and is the dominant feature which such registers exhibit at the system terminals.

The storage unit is said to be *erasable* if it is possible to enter data into the storage unit (both originally and into already used storage registers) under the control of the parent system. That is, if both the write and the read phases of the operations are permitted, then the memory is said to be erasable. Usually in such storage units the write phase will require roughly the same elapsed time as the read phase. If the write phase requires considerably more time or requires intervention by the operator, the storage unit is often said to be *changeable*.

Nearly all of the high-speed storage units, such as those designed around the magnetic core storage on the left in Fig. 2, are erasable. Indeed it is as easy to write new data into them as to read from them; hence, such storage units are often referred to as "scratch pad" storage by computer users. Most of the back-up storage units are also designed to be erasable; in the case of magnetic surface storage (as in drums and discs) it is possible to pre-record them and supply them only with reading equipment so that they are no longer erasable. Indeed it is easier to think of the few examples of storage units which are not erasable than to cite the many which are.

The storage unit is said to be *fixed*[8] if the data are essentially built into the storage registers and cannot be changed without a major revision in the equipment. Users term such memories "recall" or "read-only" storage units. They are used primarily to save the expense of the write equipment of erasable memories and to avoid the danger of accidental erasure. There is little essential difference between such a system and

a signal recoder (decoder-encoder) except in size. Such storage units are constructed by presence or absence of diodes, capacitors, etc. at the intersections of digit lines and selection lines (see Fig. 5). They are also constructed by permanent wiring—for instance, an entire word may be stored in a single core where the information is stored by having the digit line link or not link this core. This type of storage unit is becoming much more important for very large capacity stores as it can generally be produced at a lower cost per bit.

The storage unit is said to be *volatile* if the stored data are vulnerable to loss through power failure or other mishap. This does not, of course, include the mistaken use of the write command as a mishap. From the terminals of our conceptual model, all volatile stores must be considered erasable. However, a distinction is made in that the user may replace data if the loss of data through volatility is critical.

The most common volatile storage units employ electrical or ultrasonic delay lines. The most common examples of the latter type of course are the magnetostrictive and fuzed quartz delays. Such storage units are very economical and reliable; with reliable power sources the volatility is not generally considered to be a drawback. Indeed, it has recently been shown that it is possible to design magnetostrictive lines as fixed rather than volatile stores. Cryogenic storage units must also be considered volatile to power failures that last long enough for ambient temperature to rise above the superconductivity region.

REFERENCES

1. J. Goldberg, MIRF (Multiple Instantaneous Response File) Quarterly Reports, AF 30(602)-2142 Contract RADC.

2. W. L. McDermid and H. E. Petersen, "A Magnetic Associative Memory System," *IBM J. of Res. and Dev.*, Vol. 5, No. 1, pp. 59-62 (January 1961).

3. Burroughs Corp., Mfg. literature describing B5000 computer (1961).

4. J. C. Shaw, A. Newall, and H. A. Simon, "A Command Structure for Complex Information Processing," Proceedings Western Joint Computer Conference 1958, pp. 119-128.

5. Edward Fredkin, "Trie Memory," *Communications of the ACM*, Vol. 3, No. 9, pp. 490-499 (September 1960).

6. M. M. Astrahan, "The Role of Large Memories in Scientific Communications," *IBM J. of Res. and Dev.*, pp. 310-313 (October 1958).

7. W. W. Peterson, "Addressing for Random-Access Storage," *IBM J. of Res. and Dev.*, Vol. 1, pp. 116-129 (April 1957).

8. "Fixed Program Storage Techniques," ASTIA Report AD 145107.

III DISSECTION OF THE CONCEPTUAL MODEL OF A STORAGE UNIT

A storage unit can be represented by a single conceptual model and classified into many kinds from its terminal characteristics alone. However, to fit the general definition of a storage unit, each of these kinds can be internally divided into four fundamental parts: (1) the storage medium itself, generally arranged in an aggregate of storage registers; (2) an access technique to couple the input address register to the desired storage register; (3) a sensing technique for determining the data stored in the selected register and transferring data to the output register; and (4) an organizational scheme to provide the controls and basic equipment which permit the functional parts to produce the desired operation.

A. THE STORAGE MEDIUM

The fundamental requirement of the storage medium is the retention of the digital data received from the parent system. Since no method has been found to be more reliable than binary circuits for the handling of digital data, the storage is usually also in binary or coded binary form. Storage of a single binary digit or bit can always be provided by any material, device or circuit which can be made to display a hysteresis loop in its plot of response versus excitation. The necessary material, device, or circuit component that stores a single bit is called a storage cell. Such cells are arranged in groups. The number of cells per group corresponds to the number of bits in a basic word of the parent system and storage unit. Such groups are defined as *storage registers*. One unique register corresponds to each unique address of the storage unit.

Besides the number of cells in a storage register, there are five important attributes which are useful in classifying these registers. These are (1) the basic storage mechanism; (2) the physical nature of the storage media; (3) the permanence of stored information; (4) the nature of the connection with access and (5) the form of energy supplied by access. This classification is summarized in Fig. 3.

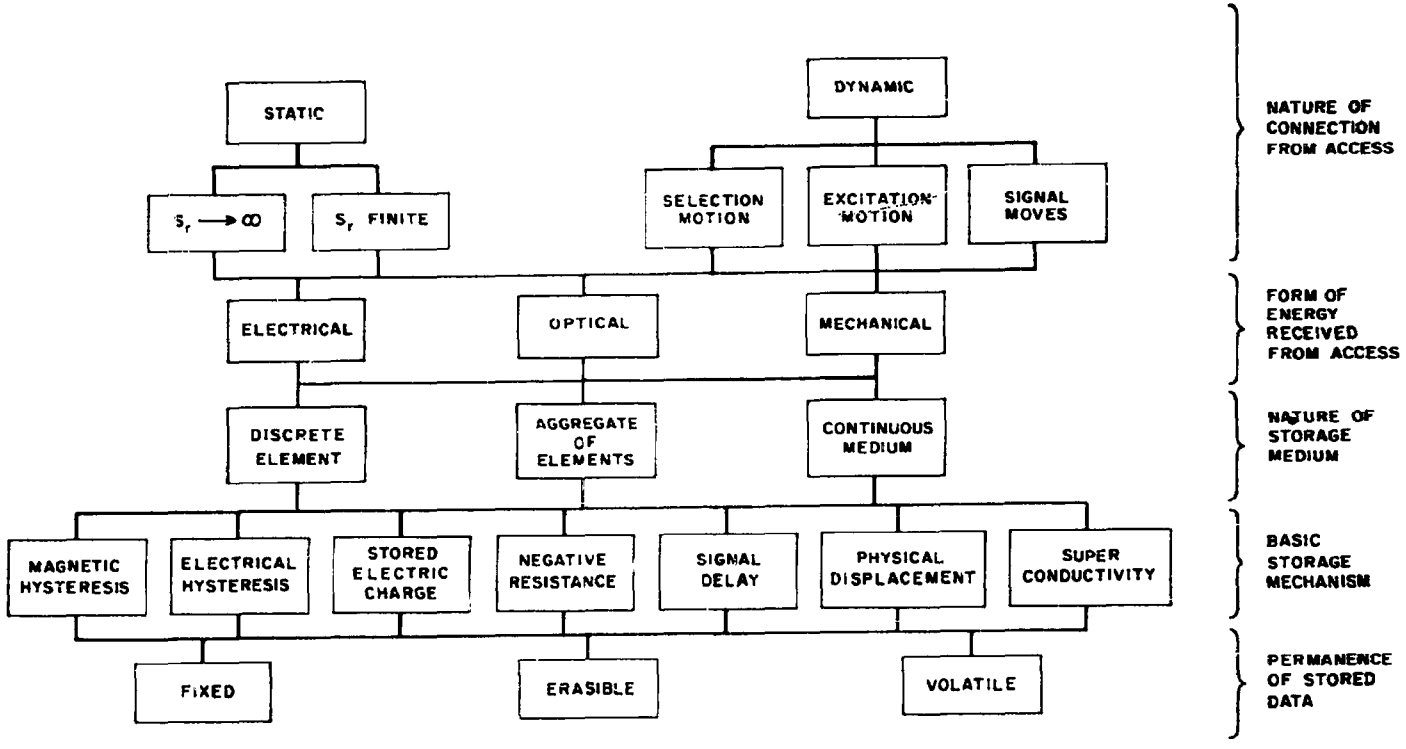


FIG. 3

CLASSIFICATION GRAPH OF STORAGE REGISTERS

1. Basic Storage Mechanisms

a. Magnetic Hysteresis

Magnetic hysteresis as displayed in ferromagnetic materials is by far the most frequently exploited basic mechanism. All but a very few storage units in working computers today exploit this phenomenon in one way or another. A large amount of basic work has, therefore, been done to understand magnetic phenomena and detailed accounts may be found in many texts.[1,2,3,4] Briefly, if a magnetic field of intensity H is applied to a given volume of ferromagnetic material, the induced magnetic flux density, B, will be many times greater than its value in air.[5] Furthermore, increases in the value of the magnetic field intensity will eventually saturate the magnetic flux density in the material, and further increases in H will not affect B. Upon removal of the applied magnetic field, the magnetic flux density in the material does not drop to zero, instead, a certain amount, B_r, remains as remanent flux density, providing a natural stable state. A magnetic field intensity must be applied in the negative direction in order to return the magnetic flux density to zero. Further increases in magnitude of the applied field in the negative direction will reach a saturation flux density in the negative direction; again, upon removal of the applied field, a remanent flux density of $-B_r$ will remain in the material, thus producing the familiar $B - H$ loop.

Several special features make magnetic hysteresis especially attractive in digital storage. First of all, the two stable states mentioned above are natural or static stable states, *i.e.*, they require no stand-by power in order to maintain their remanent states. Secondly, magnetic storage registers are nearly always constructed from relatively inexpensive materials. These materials can be designed to display a very good threshold, *i.e.*, a sharp nonlinearity in the response-*vs* excitation curve. Devices of these materials can be made extremely reliable and resistant to the environment (with the exception they must remain well below the Curie temperature). Magnetic phenomena can yield very high speeds or very high storage densities with considerable latitude for compromise to achieve a particular state.

These properties are realized in a wide variety of devices and geometrics. The magnetic core, presenting a closed flux path, is by far the most common method of exploiting this storage mechanism in high-speed, erasable storage units. Switching from one stable state to the other is

achieved by passing a current on one or more wires through the aperture of the core to produce a magnetomotive force sufficiently above the threshold. Reversible switching to the opposite state is achieved by reversing the direction of the current. Speeds achieved range from a small fraction of a microsecond to several microseconds. The switching speed is a function of the magnitude of the applied field and is inversely related to the amount or volume of material switched. A most common way of determining the remanent state of the core, as in reading, is to apply an excitation field in the direction that switches the core to the zero or reset state. If already in the zero state, little or no switching occurs and relatively small output voltage is induced in the sense circuitry. If in the one state, complete switching occurs, inducing relatively greater output voltage in the sense circuitry. Thus, the act of reading destroys the stored data, producing a destructive read-out. Sufficient circuitry must be applied to rewrite the data after reading. The ratio of the induced output voltages for *ones* and *zeros* depends upon the volume of switched material and on the speed and temperature of the core. If this excitation energy for core reading comes from a single source or dimension(see Section III D-2) the magnitude of the field may be made very large compared to the threshold in order to reduce the switching time. This is typically done in linear-select[6,7] storage units. However, if the excitation energy comes from two or more sources, and each source links other registers, thus producing partial excitation in unselected registers, this partial selection must remain below the threshold field, and the overdrive be limited to a small selection ratio.[8] The most common core sizes are the 80 mil. outside diameter by 50 mil. inside diameter and the 50 × 30 mil. cores. While smaller sizes produce higher speeds, there is a physical limit to the reduction in size that can be handled in practical situations. Memories are now becoming available with a 30 × 17 mil. core, which appears to have sufficient mechanical strength. Packing densities of wired-core storage registers range from a few thousand to a few million per cubic foot.[9] While unwired cores cost only around a cent per bit in very large quantities, when they are incorporated in finished storage units with access circuitry the cost generally rises to a few tens of cents per bit. This moderate cost, the high reliability, and the simplicity of system concept have contributed to the exploitation of magnetic hysteresis in this form.

Many schemes have been devised and employed for improving the characteristics of core storages in one form or another. Using two cores per bit has increased the speed, increased temperature tolerance and

equalized the load on access outputs.[10,11,12] In some instances it has provided for nondestructive read-out. Complex device configurations and multiple flux paths have been used to achieve various advantages. The three-hole transfluxor,[13,14,15,16] MAD,[17] and Biax[18] all permit higher speeds and nondestructive read-out at the expense of increased cost per bit in the storage register.

Another common method of exploiting magnetic hysteresis is in elemental saturated areas of a magnetic surface producing an open flux path. Magnetic theory assumes continuity of flux lines, which establishes a demagnetizing field in air to permit sensing of the remanent flux state without acutally switching it. This is usually done by passing a probe or reading head through the demagnetizing field.[19] Thus, the excitation energy for the selected register is the mechanical production of a rate of change of flux which induces a voltage capable of being sensed in the probe or read head. This operation produces a non-destructive read-out which can be electrically altered by passing a current through a similar (or the same) head at the appropriate time and in the appropriate direction.

This process is exploited by applying a coating of ferrite materials under 1 mil. thick onto a supporting surface for easy transport to the vicinity of the read head (as in drums, discs and tapes). Although magnetic drums have been used for the high-speed working storage unit of some relatively slow machines, their longer access time relegates them primarily to the role of back-up storage units. There are a wide variety of techniques for representing primary bits (*ones* and *zeros*) in the remanent flux density of a magnetic surface. These include, of course, positive remanance for *one* and negative remanents for *zero* in both return-to-*zero* and nonreturn-to-*zero* schemes. There are also many techniques for using flux reversals to represent primary values rather than flux densities. A good review of the available schemes can be found in the available literature.[4,20,21,22]

The main reason for using storage in a magnetic surface of this type is the far lower cost per bit than in high-speed storage units. In drum and disc access of a given storage capacity, costs run from a small fraction of a cent per bit to a few cents per bit (generally about one order of magnitude less than high-speed storage units). In tapes, punched cards, and so on, the storage capacity is unlimited when manual storage on

a shelf is included. However, for single reels, tape stations can achieve a cost per bit of as little as one hundredth of a cent. Since switching in the storage cell does not constitute a portion of the access time, the read access time is limited only by the access circuitry. The mechanical speed with which read head and storage register can be brought together, and the maximum frequency limit of the sensing equipment, are the limits on speed. Packing densities are generally quoted in bits per square inch of surface and in bits per linear inch under a single head. Practical limits now seem to be approximately one thousand bits per inch or a few tens of thousands of bits per square inch. The Laboratory for Electronics HD file drum achieves 22,000 bits per square inch. Laboratory experiments have shown that more than 3,000 bits per inch are possible under single heads which can be stacked 500 to the inch.[20] It is theoretically possible to exceed this figure by an order of magnitude.

Many new geometries and driving techniques have recently been introduced. Most of these have been aimed at reducing the volume of switched material, either physically or electrically, in order to increase speeds, reduce energy dissipation, and reduce fabrication costs. The "twistor" magnetic rod, "tensor" Biax devices and the impulse and partial switching techniques are examples of this.

Very great increases in speed of switching have been demonstrated in devices exploiting the rotational mode of switching. In these devices the entire magnetic domain is rotated to the new orientation simultaneously, as opposed to domain wall motion. Rotational switching is generally realized in thin film spots,[23,24,25] cylinders,[59] and sheets[26] of a nickel-iron alloy similar to Permalloy. Also, the Fluxlok technique[27] demonstrates one example of high-speed rotation in ferrite cores. The switching time of these devices is limited *only* by the rise time of the excitation energy.[27,28]

The "Curie point" effect provides another interesting way to store data in magnetic medium. The entirety of a thin continuous film of material is magnetized to saturation normal to its surface. An electron beam is then allowed to impinge on an elemental area (approximately 0.0002 inch in diameter) of the film. The temperature of the spot is thus raised above the Curie point to effectively demagnetize the area. Read-out can be effected either electrically by electron mirror microscope or optically by the Kerr magneto-optic effect.[77]

b. ELECTRICAL HYSTERESIS-FERROELECTRICS

Ferroelectric materials are a class of ionic compounds with dielectric properties which are in many ways analogous to the properties of ferromagnetic materials, that is, they exhibit electric hysteresis in polarization *vs.* electric field intensity. It is this analogy and not the composition of the materials which accounts for the name. Devices have been fabricated both from artificially grown single crystals and from polycrystalline ceramics of either single ferroelectric compounds or mixtures of compounds. Thin films of ferroelectric materials have also been fabricated. Interest in ferroelectrics for digital storage was stimulated by their potentially small size and planar geometry which permit many devices on a single substrate and by the large output signals available. Storage in these devices can be accomplished by coincident voltage and readout either by voltage pulses or RF sensing. Ferroelectric also offer some possibilities for operation at higher temperatures than ferromagnetics but suffer from the usual circuit disadvantages of a two terminal device.

Device and storage system development has been disappointing, largely due to the instability of available materials and the lack of a true threshold field. Many new materials have become available in recent years and some offer hope of overcoming some of the difficulties[29] but they are still a long way from useful engineering materials. Switching speeds probably will never be as fast as ferromagnetics unless extremely thin ferroelectric films can be developed, because ion displacement is inherently a slower process than spin rotation. However, the high impedance and nonlinearity of ferroelectric devices have been advantageous in conjunction with electroluminescent storage and display devices.[30]

Somewhat akin to the remanent dipole storage of ferroelectrics is the persistent internal polarization storage in phosphorus.[31]

c. STORED ELECTRIC CHARGE

The fact that capacitors can be built with extremely low leakage gives the possibility of providing reasonable long-term storage by merely charging a linear capacitor. However, since such a device does not have natural stable states, artificial amounts or levels of charge placed on the capacitor must be *defined* as representing required *ones* and *zeros*. Likewise, since the leakage current cannot be made identically *zero* a mechanism must be provided to periodically recharge the capacitor. No nonlinearity is

inherent in such a device, therefore additional devices must be associated with the individual storage cells to achieve hysteresis between response and excitation. A notable example of the use of linear capacitors in storage is the diode capacitor store;[32] here the nonlinearity is supplied by small diodes and the storage by the capacitor. This storage unit had the advantage of being extremely fast, but was too expensive for general use. In the barrier grid store,[33] the nonlinearity is supplied by the ability to control the electron beam to charge elemental areas of the phosphor through the grid. Both such stores were used in early computers, but were found to be more expensive and more difficult to maintain than the ferromagnetic core and are no longer generally used.

d. NEGATIVE RESISTANCE AND GAIN NONLINEARITY

A hysteresis loop in the response-*vs*-excitation characteristic can be artificially produced by the suitable combination of linear and nonlinear circuits elements. Many two-terminal devices can be combined with a power source and linear resistance whose load line intersects the device characteristic to produce the two stable states. These states are not natural or static in that some power must be drawn continuously from the source to maintain them. Devices of this type are termed *negative resistance elements*; examples include the neon bulb,[34] the tunnel diode,[35] and the Cryosar.[36] Several three-terminal devices can be arranged into flip-flop circuits having similar characteristics, typically vacuum tubes and transistors. Such circuits are said to employ gain nonlinearity.

The principal advantage of circuits exploiting these storage mechanisms is the speed of response. Generally speaking, the cost of storage in these circuits (several dollars per bit) is far too great to consider for very large capacity storage units. However, compatibility of input/output signals from registers employing these circuits with the signals used in logic circuits, and the high speed of circuit response make them very useful for the few storage registers within other units of the parent system and as input/output registers for storage units.

The extreme speeds (switching speeds less than one nanosecond) of tunnel diodes and their very small physical size has led to considerable effort to design reasonably large capacity, extremely high-speed memory around these devices.[37] However, the problems of sensing the stored bit and the very high cost per bit of storage cells designed around these elements have not yet been suitably solved.

Relays were among the first devices exhibiting gain to be used as storage cells and the logic elements of access equipments. Their slow speeds compared to other available devices has made them essentially obsolete. New interest in relay circuitry as a storage mechanism has been generated by the possibility of manufacturing microminiature relay devices with electron-beam-machining.

e. SIGNAL DELAY

A very useful mechanism for achieving storage takes advantage of the delay time inherent in the velocity of propagation of signals.[38,39] This includes electric delay lines, in which the signal energy remains in electric form.[40] In these lines the velocity of propagation and the Q of the line preclude the storage of more than a few bits. Hence their most important use has been in single-bit storage for dynamic flip-flops.

Much more important are the so-called acoustic or ultrasonic delay lines. In these lines the signal energy is converted to a mechanical stress by a write transducer at the input and reconverted to electrical energy by a read transducer at the output. Early media used included quartz and mercury tanks in which the data were transmitted as bursts of 1- to 2-Mc energy (hence "acoustic" is a misnomer). The propagation delay and Q of these lines permitted a few hundred bits per channel. Such lines were, however, very sensitive to temperature.

Magnetostrictive delay lines are the most common means of exploiting signal delay in currently available storage units.[41] Such lines are essentially a rod or wire of an iron-nickel alloy which tends to change its physical dimensions in a magnetic field. Thus the write/read transducers are merely solenoids to produce the pulsed magnetic field. Bit information is propagated as single (or double) pulses of mechanical stress rather than bursts of high frequencies. Both the line and the associated circuitry are comparatively simple, reliable, and inexpensive. Hence, such lines have become the primary storage in many low-cost systems whose operating speeds can tolerate the cyclic access (therefore similar and competitive with magnetic drums). Although this mechanism is inherently volatile, the ability to place many sense coils (read transducers) along the line has led to several fixed storage techniques with magnetostrictive lines.[42]

Another type of signal delay which has not yet been fully exploited is spin echo.[43] The data are stored using the nuclear spin phenomenon of organic materials in a strong stationary magnetic field. Data are entered via a solenoid around the material and are retrieved from this coil following a recall pulse. The pulses are returned in a mirror image (i.e., last-in, first-out) in time about the recall pulse. In general, this format and timing are not conducive to digital computer storage. A more serious disadvantage is that data can not be re-entered immediately on reading, since a settling time is required before re-use.

f. PHYSICAL DISPLACEMENT OF MEDIA

Physical displacement of media can take two principal forms: the presence or absence of material and the motion or deformation of material. The presence or absence of material, such as punched holes in paper tape, has found much greater acceptance in input/output units than in internal working storage units in a computer. However, the presence or absence of deposited silver, as in a photographic plate, with the feasibility of storing more than a million bits per square inch, has held great promise for high-speed fixed stores. The means of accessing and determining the presence or absence of a particular bit or group of bits in such high-density storage is a problem not yet solved economically. The two most successful attempts to exploit the high-density possibilities of photographic film or plates have been the flying-spot stores developed at Bell Laboratories[44] and the Photoscopic Disk Reader developed at IBM.[45] In neither of these systems is the capacity limited by the ability of photographic films to resolve spots. The limit is, rather, imposed by the ability of the flying-spot scanner to produce and position the light spots in the phosphor with sufficient brightness and accuracy. The spot brightness is limited by the risk of burning the screen; techniques for rotating the tube face have been employed to move the spot over the phosphor to prevent burning while still holding it in a fixed position relative to the storage. Both of the above systems employ a servo loop around the spot-positioning circuitry in order to achieve the required accuracy.

The permanent magnet twistor storage units[46] relied on the presence or absence of small permanent magnets glued to a replaceable card for data storage. There have been many one-dimension, read-only

storage units which used the presence or absence of a wired-in diode at the intersection of word selection lines and digit lines to provide storage of fixed information. Two very closely related schemes are the Card Capacitor Store developed at IBM[47] and the Ferrite Rod Store developed at Ferranti, Ltd.[48] These storage units use the presence or absence of capacitors in the former and inductors in the latter to modify the coupling at these intersections.

The deformation of material is principally found in the relatively new thermoplastic recording.[49,50] Briefly, this technique involves depositing electric charge on the thermoplastic material in accordance with the desired information pattern. The material is then softened thermally and equilibrium of forces (electric and surface tension) deforms the surface which is then refrozen. The principal means of reading out the stored information takes advantage of the differential defraction which the distorted surface causes to a collimated beam of light in a Schlieren optical system. While it is conceivable, using electron optics, to lay down as many as eighty million bits per square inch,[51] if the read-out is to be optical, the limitations on storage density will probably be similar to those on photographic stores, which are limited by the light source or flying-spot scanner. One principal advantage of thermoplastic recording over photographic recording in systems of this type is the electrical changeability. However, to erase and change a given bit requires heating and softening a large number of bits in a given area, and the time required to do this is considerably longer than a read-out cycle.

g. SUPERCONDUCTIVITY

In many metals, alloys, and compounds whose temperature is reduced to a point somewhere between 0°K and 18°K, all detectable electrical resistance abruptly disappears.[52,53,54] This phenomenon is termed superconductivity, and the materials which display such abrupt disappearance of electrical resistance are termed superconductors. The temperature at which this phenomenon occurs in different materials is termed the critical temperature, T_c. If a current is induced to flow in a superconductor, the current will persist, since there is no electrical resistance and will be a *supercurrent*. The existence of a magnetic field decreases the critical temperature for the portion of material in the magnetic field, which produces a control over such persistent supercurrents. This phenomenon has

been most heavily exploited for purposes of achieving logic, and storage cells of many logic elements are possible. However, a basic superconductive memory element termed the *Crowe* cell or *trapped-flux* cell has been described.[53,54] Such cells can be organized into a two-dimension read-storage unit in an organization similar to the coincident-current memory using magnetic cores. Superconductors have one tremendous advantage over magnetic cores. The fact that the electrical resistance is absolutely zero, means that there is no noise problem from half-select cells, which is one of the principal limitations to increasing the capacity of core memories. Limitations on superconductors have come in two forms. When the devices are made large enough to be easily produced and handled, the L/R time constants turn out to be inordinately long and conversely when time constants are compatible with high-speed computers (as in thin film devices) reliable production methods have not been found.

h. PHOTOCHROMIC

Photochromic storage phenomena may be considered a reversible photographic system, in which three separate wave lengths of light are employed. (one to write or initiate high absorbance, the second to read or sense the absorbance and a third to erase or eliminate the high absorbance). Photochromic storage cells have been made in the laboratory from certain organic compounds whose absorbance to a particular wave length of light may be switched to a very high value by previous illumination. This is a reversible process in which the absorbance is erased by subsequent illumination at a different wave length.

Densities in excess of 10^6 photochromic cells per square inch appear practical for storage However, all the problems of access to photographic storage are encountered plus the additional need for variation in wave length of the light source.[76]

2. PHYSICAL NATURE OF STORAGE MEDIA

It is helpful in understanding a particular memory system to identify the portion of the system which belongs with storage and that which belongs with access or sensing and read-out equipment. One classification attribute that is helpful in identifying these storage registers themselves is the physical nature of the register or cell.

a. AGGREGATE

Many of the basic storage mechanisms discussed in the last section are most easily exploited when several circuit elements are aggregated to provide storage of a single bit in a single cell. This is, of course, required in all gain-nonlinearity and negative-resistance devices. Methods of increasing the speed of magnetic core cells have been described which used two cores per bit, making a circuit aggregate of a single cell. Aggregates of circuit elements are generally expensive, both because they use more elements and because they require more wiring interconnections than discrete elements. Aggregates are generally used in order to increase the speed, reliability, or both of a particular storage unit up to approximately 10^4 bits. Very large capacity memories generally do not employ circuit aggregates for a storage cell because of the high cost. This may not, however, be true in the case of crosspoint cryotrons, whose individual cost promises to be very low, permitting a superposition of logical capability onto storage in a single cell aggregate of circuit elements.[55]

b. DISCRETE ELEMENTS

The storage media may be termed discrete when one and only one distinct circuit element provides complete storage function for a single cell. Thus a collection of N such elements would provide a storage register for an N-bit word. Typical examples of this would be the one-core-per-bit magnetic core storage units. Other examples are to be found in the wide variety of linear-select permanent memories in which a diode or other such element modulates the coupling between a word-select wire and the information leads. Many high-speed, random-access, erasable memories are now constructed with discrete storage elements. It has often been pointed out that as the storage capacity is increased, the fabrication and wiring of a discrete element for each bit becomes unduly costly. For instance, if one second is required for the fabrication, testing, and wiring of each individual storage cell of a one-billion-bit storage unit, 33 years are required for its completion (*i.e.*, one gigasecond is equal to one-third century). However, storage units of approximately 10^6 or 10^7 bits have been designed around discrete storage elements. It is a matter of choice in some systems how much is included in the storage cell and how much is considered a part of the access or read-out equipment. For instance in a permanent-magnet twistor memory system, the permanent magnet can be

considered a discrete storage cell, and the twistor, information lines, and drive solenoids can be considered a part of the access and read-out equipment. Conversely, the elemental portion of the twistor information line associated with the permanent magnet can be considered a part of the storage cell, in which case the storage cell becomes an aggregate of circuit elements.

c. CONTINUOUS MEDIUM

The achievement of very large capacity storage, *i.e.*, in excess of 10^7 bits, has almost always been through the use of a storage cell formed in an elemental area of an apparently continuous medium or surface. The principal examples are, of course, magnetic tapes, drums, and discs. In these forms only cyclic and serial access are possible. Random access to a continuous sheet of gyralloy material, through printed-circuit windings has been demonstrated[26] in a very high-speed thin-film store. Pseudo-random access is achieved through the use of a flying-spot scanner to photographic and thermoplastic media in continuous form.

3. PERMANENCE OF STORED DATA

The permanence of stored data relates to the ease or difficulty of maintaining and changing the information within the storage registers. It is the principal attribute of the storage registers to make itself felt at the terminals of our conceptual storage unit. It is a convenient way of classifying storage registers.

a. ERASABLE STORAGE

If the stored data within the storage registers may be changed at will under the control of the parent system, the storage is said to be *erasable*. The great flexibility of the stored-program computer is largely due to the ability to build erasable storage units. Many of the discrete, hysteretic circuit elements used in the construction of storage registers are sensed by switching them to a *zero* or reset state, as in many of the magnetic-core and thin-film memories. The very process of switching to the reset state erases the stored information, placing the storage registers in readiness to reinsert data. Such action is termed destructive read-out. For long-term storage, a write cycle normally follows immediately after a read phase, and the information is taken

from the output register and reinserted in the storage registers. The circuitry for such automatic rewriting is normally included within the storage unit, so that destructive read-out storage is not directly felt at the terminals. Indirectly, however, it increases the read cycle time over the read access time by requiring the added write cycle; such memories are normally said to require a given number of microseconds for a complete read/write cycle.

There are many erasable storage techniques aside from the destructive read-out techniques. Some of these involve special techniques in switching cores, or in adding an aperture or core to provide more than two stable states. With three stable states it is possible to switch to a reset state from either a stored *one* or a stored *zero* state. This technique is used in transfluxors, in several two-core-per-bit memories, as well as in tunnel diodes and in Cryosars.

Storage on a magnetic surface is generally made erasable. Since the process of reading involves no switching of magnetic material, erasability can be incorporated merely by including circuitry for writing. Some drum storage units, however, are written into when constructed and delivered with read capability only.

b. FIXED STORAGE

The storage unit is said to be *fixed* or permanent if the parent system cannot alter the stored information. The two major advantages of such storage are (1) invulnerability to loss through erroneous commands and (2) the possibility of using techniques that cost less than those required for erasable storage. One example was cited in the last paragraph where fixed storage is obtained by the simple expedient of omitting the write circuitry in storage on a magnetic surface. A much more common example is in the linear-select memories in which the couplings between the selection lines and the digit lines are modified. The two best known examples of this are the capacitor memory of IBM[47] and the ferrite rod store of Ferranti, Ltd.[48] In such static-access memories, speed is gained not only through the omission of a write phase, but also through the omission of any elements requiring switching or turnover time.

Many fixed stores can be changed only by making a major change in the construction of the unit. Others can be changed readily by altering

some small portion of the unit. This is the case with the Bell Labs. flying spot store, which requires merely the changing of the photographic plates with the stored information. The plates cannot be changed by the parent system, and it is therefore classified as a permanent storage unit. The Bell Labs. permanent-magnet twistor store falls in this same category. The cards containing the permanent magnets must be removed and replaced manually, which is relatively easy. The IBM photoscopic store[45] with photographic rotating disc which must be replaced to change the stored data is another example of this particular class.

c. VOLATILE STORAGE

If a storage register is subject to loss of the data contents either from power failure or from passage of time, it is said to be *volatile*. There are two categories of volatility: *periodic* and *aperiodic*. Periodic stores must be regenerated within a given period of time (*e.g.*, condenser diode stores, in which power must be added to make up for the gradual leakage of charge from the condenser). This is also true of the target potential stores such as the Williams tube. All delay-line stores must also be periodically regenerated—in fact the period of regeneration is identical to the storage time. Storage mechanisms such as negative-resistance, gain bandwidth, and superconductivity are subject to loss through prolonged power failure and thus, from the terminals of a storage unit, must be considered volatile.

4. NATURE OF THE CONNECTION BETWEEN THE STORAGE REGISTERS AND ACCESS EQUIPMENT

This connection plays a strong role in determining the permissible storage elements and the speed of access to them.

a. STATIC CONNECTION

If each storage register is directly wired to the access equipment so that no mechanical motion is involved, the connection is said to be *static*. Virtually all of the storage units shown in the high-speed group on the left of Fig. 2 employ a static connection. The great advantage is, of course, speed of access to the stored data.

There are two major types of storage registers capable of static connection: (1) those requiring complete external selection and (2) those

permitting partial internal selection. Complete external selection means that the storage registers do not take part in the decoding of the address input, and the read selection ratio (see Section III-D-2) approaches infinity. This type of connection has been given many different names in the literature, such as word-organized, linear-select,[7] end-fire,[55] switch-driven, and set-a-line[57] techniques. All of these names imply that essentially no energy is permitted on the access connections of the *unselected* storage registers, which would require these registers to determine for themselves whether or not they are selected. There are many examples of storage units employing this type of connection, such as the Bell Labs twistor store,[58] the National Cash Register rod memory,[59] and various linear-select magnetic-core memories at Lincoln Laboratories.[7]

Partial internal selection requires the storage registers to take part in the decoding or selection process, *i.e.*, the selection ratio is a ratio of small whole numbers. Such is the case, for instance, in the popular coincident-current magnetic-core storage units. In this type of storage unit each output connection from the access equipment supplies partial excitation energy to a large number of storage registers. However, in only one register do the partial energies combine to full excitation. This requires the storage cells to have a sufficiently sharp threshold characteristic to distinguish between partial and full excitation energy. Magnetic cores have served sufficiently well in this regard to be the most used design technique in commercial high-speed storage units and to be the scheme used in the Lincoln Laboratories TX-2 S unit, which is the largest capacity static access unit (single module) known.

Many techniques are available for increasing the selection ratio in order to decrease the read-access time, the tolerance to current variations of the drive currents, or the tolerance in parameter variation in the cores.[60,61] It is interesting to note from Fig. 1 that such memories offer the best chance of achieving one-billion-bit capacity with only a few microseconds for access.

b. DYNAMIC CONNECTION

Access involving mechanical motion of some type in the connection between storage register and access equipment is said to be *dynamic*. While

mechanical motion generally increases the read access time over static access, it is considerably less expensive to implement. There are three principal ways in which motion is involved in access:

(1) Either the storage register or the access equipment physically move into the proper position to couple the desired storage register to the read/write equipment. Once in position, the reading or writing occurs without further motion. Examples of this are the flying spot scanner in conjunction with the photographic plate store or thermoplastic store, *i.e.*, the motion is required only for selection not for the read/write excitation. The Williams tube store[62] also uses this technique. The electron beam is moved into position, after which reading and writing is possible.

(2) Relative motion is required between the storage register and the access technique in order to induce the proper voltages to achieve reading. The most common example of this technique is storage in magnetic drums, discs, and tapes,[19] where it is the motion of the storage medium past the read head, so that the flux lines of the demagnetizing field in air are cut by the read head, which induces the voltage in the read head. Thus, read excitation and selection are both supplied by mechanical motion. It is not, however, true that the same motion is required for writing.

(3) The desired signal moves with finite velocity through the storage medium, the access is thus a time coordinate and a clock must be provided to know which storage register is currently being read out of the read head. Examples of this are ultrasonic delay and magnetostrictive delay lines.[41,42]

5. Form of Energy from Access

The excitation energy for either reading or writing can enter the storage cells in a variety of forms.

a. Electrical Energy

For all static-access storage units, the excitation energy is electrical. The most common units are the current-driven storage registers such as magnetic cores, thin films,[24] twistors,[63] and plated rods.[50] The excitation energy is in the form of electric current, either pulses or a

change in level. Ferroelectric cells[64,65,66] and the IBM capacitor stores,[67,68] on the other hand, are excited by essentially voltage sources. The energy from an electron beam forms the most common dynamic connection through which the storage registers receive electric energy from access.

b. OPTICAL ENERGY

Photographic and thermoplastic storage generally require that the excitation energy be converted to an optical energy (radiant energy in or near the visible spectrum) for use in selecting the desired storage register. Storage involves permitting or preventing the passage of this selection energy (in optical form) through the storage cell to the sensing equipment. The most common way of achieving this at present is through the use of a flying spot scanner. The use of high speed rotating mirrors is, however, being investigated.

c. MECHANICAL ENERGY

The most common method of reading the stored data from the magnetic surfaces of drums, discs, or tape is to mechanically pass a reading head through the demagnetizing field in space adjacent to the surface. Thus, the excitation energy for reading is mechanical.

B. THE ACCESS EQUIPMENT

The second major division of our conceptual model is the access equipment. The fundamental tasks of the access equipment are (1) to decode the input address for selection of the desired storage register and (2) to provide the excitation energy to this selected register for both reading and writing. Five convenient classification attributes are the order of access, the nature of the output, the basic physical principle, the alterability of the decoding, and the logic description. These are summarized in Fig. 4.

1. ORDER OF ACCESS

This is, of course, the same order of access in evidence at the terminals of the conceptual storage unit and was described from an external point of view in Section II. Order of access refers primarily to the mechanism whereby successive addresses are interrelated.

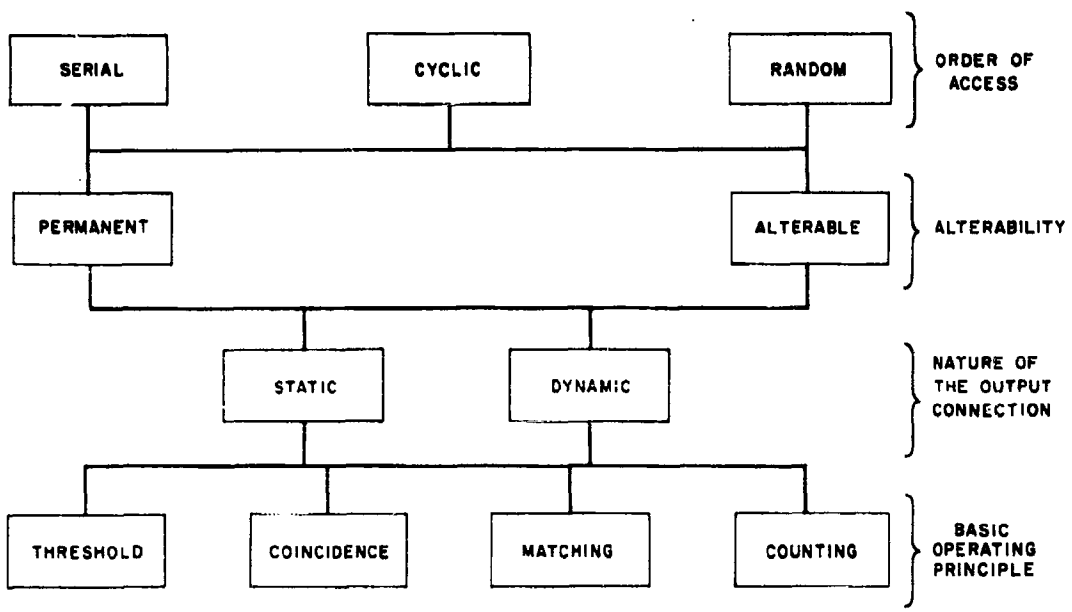


FIG. 4

CLASSIFICATION GRAPH OF ACCESS EQUIPMENT

a. RANDOM ACCESS

Random access implies that the access to the stored information at any given address is completely independent of the history of previous addresses. In order to achieve such access, complete combinational decoding is required,[@] that is, a static wired connection must be made to each storage register. There is a variety of techniques for providing such decoding and generating the necessary excitation energies. Partial or complete decoding is very often provided by diode trees or pyramids[4] (such a diode net whether tree or pyramid will be referred to here as a *matrix*). If complete decoding is done with such a matrix, then a high-gain switch or excitation driver (generally a transistor or vacuum tube) must be provided at every output to drive a single storage register (one-dimension read). Alternatively, the input to each such switch may have individual gating circuits (degenerate decoding tree) to recognize its own address. More commonly, a diode matrix is used for partial decoding to a set of excitation drivers. The decoding must then be completed at excitation power levels. A detailed study of these power level decoders appears in the Technical Supplement to this report. In coincident-current storage units (two or more dimension read) the last level of such decoding is done in the storage cells themselves. Transistor decoding trees have been used to set up a conducting path to the desired storage register with relatively slow devices; then a single high-speed driver (per dimension) provides the excitation pulse to the register via this path.

b. CYCLIC ACCESS

Cyclic access is one way of reducing the cost per bit of a storage unit by reducing the amount of access equipment per storage register. The total volume of storage registers are arranged in groups; each group shares a common channel of access equipment, and access to an individual register of the group must be separated in time. The various storage registers in a particular group are scanned serially in time. The order cannot be reversed, and immediately following the last storage register, the cycle repeats from the first storage register. The two major ways of achieving cyclic access are surface storage on rotating equipment and stress-wave propagation.

A prime example of cyclic access is the storage on the surface of a magnetic drum. The group of storage registers concerned with a single

channel of access equipment can be thought of as a single track on the periphery of the drum under this particular read head, in which case the bits of the storage register are constrained to serial read-in and read-out. Characters or words can, of course, be read out in parallel by increasing the number of tracks in a single group of storage registers. For complete decoding of the input address, some decoding is required to select the proper head(s) or track(s). This, of course, can be done by static connections to multiple heads or by mechanical motion of a single flying head along the periphery of the drum parallel to the drum's axis. High-speed circulating registers can be used in a few tracks to effectively decrease the access time of cyclic access. Magnetic discs of both rigid and pliable material have recently been added to the cyclic access repertoire, as a means of reducing the total volume and weight for a given bit-storage capacity. Rotating discs have the added advantage of much smaller amount of moving mass when used in airborne environments.

Another example of cyclic access used in modern computers is the magnetostrictive delay line in which the stored information is introduced into one end of the line by a transducer converting logic signals to stress pulses which, after traveling the length of the line, induce a received signal in a transducer at the receiving end.

c. SERIAL ACCESS

Serial access, like cyclic access, is a means of reducing the amount of access equipment per storage register from that required by static access. Access is made by linear progression from one storage register to the next. Generally, this progression can be in either direction (but not necessarily) and is essentially open-ended, permitting unlimited storage capacity by the removal and shelf storage of reels of tape and decks of cards.

The major examples of serial access are magnetic tapes, punched paper tape, and punched cards. Magnetic tape employs the same techniques for surface recording on magnetic materials as drums with two fundamental differences: the geometric shape of the recording surface is different, and the surface is generally in contact with the head, which permits higher packing densities (if skew problems can be avoided). Because of the unlimited capacity of shelf storage tapes are generally considered with input/output mechanisms or external storage.

d. PSEUDO-RANDOM ACCESS AND SLEWING IN TWO DIMENSIONS

In many instances, it is possible for dynamic access equipment to avoid the necessity of progressing linearly through the addresses of storage registers by being able either to move in two dimensions simultaneously, or to move in one dimension past groups at a time.

An example of slewing in two dimensions is the flying spot scanner, the Williams tube,[61] or any other electron-beam deflection system. With these, it is necessary to move an electron beam from one part of the screen to another in order to address a new register. The addressing of a particular register is neither completely independent of past history nor is it required to progress linearly through the available addresses.

It is important to distinguish at this time between *synchronous* and *asynchronous* access techniques. Synchronous access implies that the data output from the storage unit is always available to the parent machines at a given delay time after the control signal input, regardless of the address input. Asynchronous access implies that the parent system must remain in a state of readiness to receive the data output from the storage unit over an indeterminate period of time. Random access is always synchronous Pseudo-random, slewing, and cyclic access can be designed to be synchronous by including a buffer register for data output and making the fixed delay time after the input control signal at least as great as the longest slew or cycle time. Where this longest slew time is still short compared with operate cycle times of the parent system (as when the electron beam deflection is diagonal across the face of a Williams tube) it is practical to operate synchronously. However, where the longest slew or cycle time is much greater than the operate cycle times of the parent system, this is impractical. For instance, with a magnetic drum or disc, it would be possible to determine the fixed delay after control as equal to that of one revolution plus one word time, at the expense of reduced operating speed.

2. ALTERABILITY OF ACCESS

Alterability of the access equipment refers to the ability to change the input signals from their original appearance before use in the storage unit.

a. PERMANENT ACCESS

Fixed or permanent access is used in most storage units built today. Each unique input address can be decoded only to a given storage register, and the input data cannot be reordered before storage.

b. ALTERABLE ACCESS

For alterable access, reordering of the input signals would be possible without reconstructing the unit. The most common example of this is in buffer storage units used for format conversion. Here a plugboard is used to be able to manually rearrange the order of the data input digits before storage. Another important example is the Polymorphic Computer (RW-400) transfluxor central exchange. Here the unique storage register to which a given input address couples the parent system is dependent upon the signal routing previously established within this central exchange. That is, the decoding of a specific address to a specific storage register may be altered by the parent system.

3. Nature of Access Output

The nature of the access output is, of course, very closely related to the nature of the connection between access and storage which was used to classify storage registers in Section III-A-4. As before the major division is between static and dynamic access.

a. STATIC ACCESS

Static access refers to directly wired output from the access equipment with no motion involved. Since the excitation energy output is on one or more wires (depending on the dimensions), it is naturally electrical energy. This output energy may be a current pulse, as in magnetic core storage, or any of a variety of forms. While it may be assumed to come from a current source, it may in fact approach a voltage source so closely that "swamping" resistors must be added in the output connection to control the current amplitude. In ferroelectric storage, a voltage source is desirable from the access output. In parametron storage units, the output from access must be a quasi-continuous current of specified frequency and phase.

b. DYNAMIC ACCESS

Dynamic access refers to the use of mechanical motion to reduce the amounts of direct wiring to each storage register. This increases the average read access time, but drastically reduces the total cost of a given capacity storage unit—both by reducing the amount of access equipment per storage register and by permitting the use of many lower cost media.

There is a wide variety of ways in which mechanical motion can be used in access. The excitation energy in the access output can be electric and still be physically moved to the selected register by the decoding portion of access equipment. This is the case for any of the storage units using an electron beam as the output coupling from the access equipment to the storage register, such as the Williams tube, barrier grid tubes (and thermoplastics if a single plate is used per gun). This same mechanical motion is used for register selection in any storage unit employing a flying spot scanner; however, the access output to the storage register is converted to optical energy by the phosphor.

Alternatively, the mechanical motion can supply the read excitation energy as well as register selection. Such is the case in the most common fashion of reading from magnetic surfaces, as in drums, discs, and tapes. The read/write head is fixed in position during the reading and the storage register is moved past it, generally at a constant velocity. Heads are frequently moved into position for selection of the track or group in which the desired register is located,[70,71,72] but are stationary during reading. The constant velocity permits the final decoding to the desired register to be a time dimension. The read excitation depends on the mechanical motion and the demagnetizing field in air; however, in writing, the access equipment supplies the excitation energy and motion is used only for selection.

In delay-line storage, mechanical motion is used in quite a different way. The signal moves through the storage medium by mechanical stress waves and access is made via a transducer at one end for reading and at the other for writing. Selection of the desired register must be done in time as well as space.

4. Basic Operating Principle

Basic operating principle refers to the physical principle which is exploited in the decoding to the selected storage register. However, this physical principle is often interrelated to the method of generating the excitation energy.

A threshold is said to exist if a sharp non-linearity exists in the excitation *vs.* response curve below which essentially no response is exhibited. In exploiting such a phenomenon, it is possible to bias the device such that the threshold exists at essentially any level of exciting energy desired by the designer. An excellent example of this is the magnetic-core access switch, a very detailed analysis of which is given in the Technical Supplement to this report. Another example is the diode recoders which precede the drivers in magnetic-core access switches and the diode decoders used in many other access equipments.

A coincidence is said to be exploited if a threshold exists at a non-zero excitation energy level such that the operating level is determined by the device used in the decoding (*i.e.*, arbitrary levels are not permitted). The remanent states of the hysteresis loop are also made use of in determining the desired response. The best known example of coincidence used for decoding is in the coincident-current storage units where the last level of decoding of the input address is performed by coincidence of two or more excitation currents in the storage register itself.

The coincidence of two frequencies rather than of pulses in nonlinear elements such as magnetic cores has been used to provide the last level of decoding. In a plane of cores wired for coincident-current operation, selection is made in each direction by switching the continuous frequency to one line of that dimension. A different frequency is used for each dimension and at the storage cell common to both frequencies, the nonlinear element induces the difference frequency into the sense circuitry; the phase of this difference frequency is controlled by the remanent state of the core.[73] While no technique is known for making use of continuous frequencies for general decoding, a similar and related reading technique is employed in the parametron storage unit.[74] Here a continuous frequency excites a single word (one-dimension read) and the phase of the second harmonic is used to excite a parametron in one of two phases.

The decoding is said to be performed by matching if, in conjunction with each storage register, there is prerecorded a unique input address or its equivalent. To select the desired register, these are read out in turn and compared with the input address until a match is found. It is not essential that the storage registers be in numeric order. Examples of this process are found in many access schemes for magnetic drums[76] and magnetic tapes.

In contrast to matching, index marks may be prerecorded in connection with each storage register which are identical except in position. Thus, the decoding to the selected address is done by *counting* the number of these index marks following some master index.

5. Logical Description

The fact that the fundamental task of the access equipment has the two-fold function of decoding as well as the generation of excitation energies means that these tasks can be combined in a variety of ways.

a. DECODING LEVELS

The decoding function is generally described in terms of levels, which are the stages of the devices through which the information must pass to be completely decoded.

Single-level decoding is accomplished by providing sufficient gating at the input to the selection line (see Section III-D-2) drivers in one-dimensional read units to recognize its own unique address.[6] Decoding to these switches can be done either by trees or pyramids of diodes.

In a storage unit which uses more than one dimension in the selection of the storage register, the final level of decoding is done in the storage cells. Hence, at least two levels of decoding are required. The decoding that occurs before the generation of excitation energy requires only elements capable of carrying signal-energy levels. As many high gain switches are needed as there are decoded outputs to convert from the signal to excitation energy levels. Such switches are generally expensive and the decoding may be divided into two parts: (1) a signal recoder and (2) a power level decoder. The outputs of the recoder drive a set of such high gain switches (drivers) where the number of drivers is

considerably less than the number of outputs from the access equipment. The power-level decoder must then be provided to complete the decoding process, with elements capable of carrying excitation energy levels. This power-level decoder is discussed in great detail in the Technical Supplement to this report.

b. LEVELS OF ACCESS ORDER

Cyclic access in particular requires another order of access to couple a particular group (see Section IV) to the storage unit terminals.

c. ACCESS DIMENSIONALITY

The number of sources of energy to enter a given decoding element is designated as the dimensionality of the decoding, as opposed to the number of logic levels.

C. THE SENSING EQUIPMENT

The third major division of the conceptual model of a storage unit is the sensing equipment. The fundamental tasks of this equipment are two-fold: (1) the information stored in the selected storage register must be detected, and (2) that information must be provided as a useful data output from the storage unit. The reading process must provide for the selection of the desired register and the read excitation energy must in some way stimulate this selected storage register to provide a signal which can be detected by the sensing circuitry and is related to the stored information.

1. Sensed Signal as a Voltage Pulse

In many storage devices, the reading process generates a voltage pulse across a load resistance. Fundamentally, the voltage pulse is intimately related to the magnetic or electrostatic properties of the storage element, or to a transducer associated with the storage device.

Consider first a voltage induced by magnetic coupling to the storage element. The sense winding can be coupled magnetically to the storage cell in a variety of ways. Consider two examples, the magnetic drum and the magnetic-core matrix. In the case of a magnetic drum, the material on the

drum surface is magnetized in some desired pattern. Associated with each magnetized area is a demagnetizing field in air. As the surface of the drum moves past the reading head, lines of force are cut by the conductors of the head and a voltage is induced in the sensing circuit. The relative motion between magnetic fields and the conductor is essential in this type of magnetic coupling.

No motion is involved in sensing stored information in a magnetic-core matrix. At each storage cell, the sense lead is coupled magnetically to a read-drive lead, because both are wound on a magnetic core. The voltage induced in the sense winding by a change in magnetic field caused by current in the drive winding depends upon the permeability of the core. If the core is at the remanent state which represents *zero*, the magnetic field will drive the core into saturation. The permeability (the rate of change of magnetic flux density with magnetic field intensity = $\Delta B/\Delta H$) is very small, and little voltage is induced in the sense winding. If the core is at the remanent state representing *one*, the field will cause the core to switch. During switching, the permeability is large and a substantial voltage is induced in the sense winding.

Storage devices which depend upon magnetic phenomena in sensing information include magnetic cores, thin magnetic films, ferrite aperture plates, magnetic drums, discs, and tapes.

Consider next the voltage developed across a load resistor by a current whose magnitude and polarity depend upon the electrostatic properties of the storage element. One method of storing information electrostatically involves the controlled charging and discharging of capacitors. Holt's original diode-capacitor memory operated on this principle. Each storage cell consisted of a capacitor in series with two diodes. With the diodes held in a high resistance condition, the capacitor was charged positively or negatively, relative to a reference voltage, to store a binary *one* or *zero*. The charge on the capacitor was sensed by removing the bias from the diodes and allowing the capacitor to discharge. For one polarity of charge, one diode would carry the discharge current; for the opposite polarity, the other diode would carry the current. The polarity of the voltage developed across the load resistor indicated the magnitude of the stored bit.

The operation of the electrostatic storage tubes is basically similar to the diode-capacitor memory. A dielectric surface inside the tube is composed of many elemental capacitors, which are selectively charged and discharged by the electron beam.

In ferroelectric cells, information is stored in remanent states of polarization. A cell is read by applying a voltage step across the series combination of the cell and the load resistor. The current that flows depends upon the number of electric dipoles reversed in the ferroelectric material. If the cell is at the remanent state which represents *zero*, the applied electric field will drive the cell into saturation. The dielectric constant is relatively small and only a small displacement current flows in the load resistor. If the cell is at the remanent state representing *one*, the field will cause the cell to switch. During switching, a large number of electric dipoles reverse and a substantial current flows in the load resistor.

The following storage devices depend upon electrostatic phenomena in the sensing of information: ferroelectric cell, electrostatic tubes (Williams, barrier grid, etc.), and the diode-capacitor.

Many storage techniques require the use of a transducer in conjunction with the storage elements for the generation of a signal capable of being sensed during reading. In delay-line storage, for instance, information is stored in mechanical disturbances or stress waves which move at a relatively slow rate (compared to electronic speeds) through the delay-line medium (e.g., mercury or fused quartz). Such information is read when the disturbance reaches the end of the delay line and falls on a transducer. The mechanical displacement of the delay medium is translated in the transducer to an electrical voltage by the piezoelectric effect.

Other storage devices which depend upon a transducer to change to electrical energy in the sensing of information are: magnetostrictive delay lines, electromagnetic delay lines, paper tape (optical reading), thermoplastic tape, photographic plates, and spin-echo stores.

2. Sensed Signal as an RF Voltage

In some storage schemes, the sensing of information does not depend upon the presence or absence of a voltage pulse, but upon the presence or

phase of an RF signal whose frequency is predetermined. In these cases the sensing circuits are tuned to the desired frequency and are designed to detect the phase of the RF output signal.

The multifrequency[73] method of reading square-loop cores nondestructively illustrates the sensing of an RF signal. In reading, two RF signals, ω_1 and ω_2, are applied to the *X* and *Y* coordinates of the storage array. At the selected core, the difference frequency $(\omega_1 - \omega_2)$ is generated because of the very nonlinear *B-H* characteristic of the core and is coupled inductively into the sense winding. The phase of the RF signal in the sense winding depends upon whether the core is at the positive or negative remanent state and is 180 degrees different for the two states. The sensing circuit is tuned to $(\omega_1 - \omega_2)$; if the phase of the detected signal is the same as that of the reading frequencies, ω_1 and ω_2, a binary *one* is indicated. If the phase is 180 degrees different from the reading frequencies, a binary *zero* is indicated.

In the parametron scheme of Takahasi and Goto,[74] a frequency ω is applied to the selected *X* coordinate and a pump frequency 4ω is applied to a set of parametrons associated with the selected *Y* coordinate. Because of the *B-H* nonlinearity, a *ZX* frequency 2ω is generated in each core on the selected *X* coordinate. In each core at the intersection of the selected *X* and *Y* coordinates, the frequency 2ω is coupled to a parametron. Each parametron oscillates at frequency 2ω with its phase determined by the remanent state of the associated core.

D. THE ORGANIZATION OF THE CONCEPTUAL MODEL

1. General

While not a major division of hardware, the organization scheme of the storage unit is as important to the operation and classification as any single device or technique. The fundamental task of the organizational scheme is to achieve the desired functional operation from the interconnection of fundamental parts and the required basic equipment. Here the basic equipment includes power supplies, clock amplifiers, temperature-regulating equipment, or any other equipment required but whose function does not show directly in the fundamental operations.

Any discussion of organization must begin with a definition of terms. In general, storage units employing static access must be considered separately from those employing dynamic access.

2. Static Access Storage Units

One of the first concepts to be defined is the dimensionality of the storage medium separate from any access or sensing equipment. The *dimension* of storage is the number of sources of excitation energy for stimulation of a single storage cell. Since the excitation energy may be for reading or writing, the dimension of the storage for reading may differ from the dimension for writing. Indeed, it will be stated as a theorem without proof that the number of write dimensions must always be equal to the number of read dimensions plus *one*. It can be argued heuristically that this would be true as follows: all of the dimensions required to perform the selection function during reading will also be required during writing, plus the addition of excitation energy to carry the input data to storage.

A *memory line* is the connection between one such source of excitation energy (via the access outputs) and the storage cell. A single line may be one or more physical wires, but can only be associated with a single dimension. There are two types of lines which must be distinguished. *Selection lines* carry the energies which are the outputs of the access equipment, and *digit lines* carry the energies which are the outputs of the drivers associated with the data input (see Fig. 5).

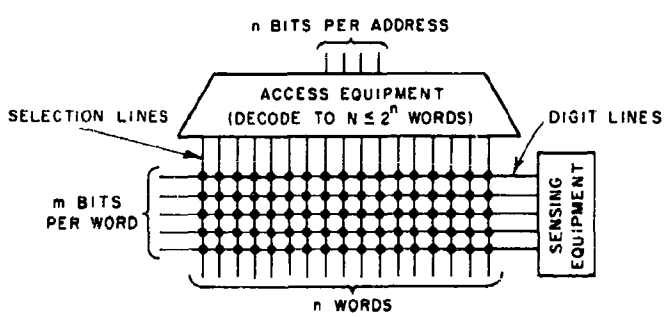


FIG. 5
ONE-DIMENSION READ-STORAGE UNIT

Hence, in a one-dimension-read, two-dimension-write storage unit, there must be as many selection lines as there are storage registers since each cell can receive energy from only a single source on read. Also there must be as many digit lines as there are bits in the data words (input data and storage registers).

Another closely associated concept is that of *selection ratio*. The selection ratio is the ratio of the magnitude of excitation energy in the selected storage register to the magnitude of the maximum excitation energy in any non-selected storage register. Thus, the selection ratio may well be different for reading and writing. It is the read-selection ratio that is used to distinguish external selection from partial internal selection in storage registers. Only when this ratio approaches infinity is it possible to drive magnetic devices arbitrarily hard in order to get very short switching times (for a given mode and switching constant). Values of 2 and 3 for this ratio are fairly common; in order to increase this ratio for increased speed, several techniques have been used in magnetic-core storage. The Technical Supplement to this report clearly shows the relationship between storage registers and the access equipment.

The *linear-select memory* is a storage unit with one-dimension read. It can be represented by a grid of memory lines as shown in Fig. 5, in which all the selection lines are in one dimension and the digit lines are in the other. A storage cell is their intersection and a storage register is thus all the intersections on one selection line of memory. The term *linear-select memory* states only that the storage registers are organized in this fashion. It says nothing explicit about either access equipment nor sensing equipment; it says nothing about what devices or techniques are used for storage; however, it does say that the selection ratio on read can approach infinity. Therefore, there need be no partial internal selection in the storage cells, and no threshold is required on reading in the cells (if access outputs provided $S_r \rightarrow \infty$); however, if the storage unit is erasable, the writing must be in two dimensions. While only a single selection line is energized, several digit lines must be. The digit lines enter all registers; therefore, the write-selection ratio must be a ratio of small whole numbers and current amplitudes need to be controlled.

If there are N registers in a linear-select memory, then there must be N connections to access equipment. Normally, one end of each selection

line is grounded and N access outputs must be decoded from an N-bit address where $N \leq 2^n$. However, if a diode or other unilateral element is included in each selection line, $N/2$ access outputs can excite pairs of selection lines with switches at the opposite end of these selection lines such that only one of the pair is grounded. Obviously, one of the address bits must be used to determine which line of the pair is to be grounded, and it is possible to use more than one bit in this way. In read-only, one-dimension storage units another saving in access equipment outputs is possible. By having a single selection line excite several storage registers, the digit lines can be so gated that only the outputs of the desired register appear in the output register of the unit.[48]

The coincident-current memory is a storage unit employing two dimensions for reading and three dimensions for writing, and therefore the selection ratios for both reading and writing are constrained to be finite. Typically, in magnetic-core storage units, the exciting currents in each dimension are one-half the full switching current, I_s. For reading, the coincidence of the two $I_s/2$ currents switches the core to the *zero* state. Writing is accomplished by applying $-I_s/2$ in the two selection dimension which tends to switch the core to the *one* state; however a digit current of $I_s/2$ may be applied on any digit line which inhibits such switching in particular cells. This scheme yields a selection ratio of 2:1 on both reading and writing. Many schemes have been advanced to increase the selection ratio in order to attain higher speeds, greater tolerance to core-parameter variation, greater tolerance to drive-current variation or all of these. A very simple way to increase the read-selection ratio to 3:1 is to apply $2I_s/3$ on the selected line of one dimension. In the second dimension apply $I_s/3$ on the selected line and $-I_s/3$ to *all* unselected lines. Thus the maximum magnitude of excitation energy in any unselected cell is $I_s/3$, which yields the read-selection ratio of 3:1. It has been shown[60] that any arbitrary ratio can be attained through special wiring and storage units[61] with very fast (less than 0.5 μsec) cycle times employing selection ratios of 4:1 and 7:1 with relatively simple wiring have been demonstrated.

•In the coincident-current memory with N storage registers, the advantage of the higher number of dimensions is the ability to reduce the amount of access equipment. In a two-dimensions-for-reading scheme, the number of memory lines (and therefore the number of connections with access)

may be reduced to something approaching $2N^{1/2}$. In general, if the number of dimensions is d, the number of connections to N registers is approximately $dN^{1/d}$. The term *number of connections* is used rather than *number of access outputs*, because it is always possible to add a diode to each line of memory involved and do some accessing at both ends (as described above) in order to reduce the number of access outputs below the number of connections.

REFERENCES

1. Richard M. Bozorth, *Ferromagnetism*, D. Van Nostrand Co., New York (1951).

2. Norman H. Scott, *Analog and Digital Computer Technology*, Chapter 11, pp. 442-509 McGraw-Hill Book Co., Inc. N Y. (1960).

3. A. J. Meyerhoff, *Digital Magnetic Circuits*, John Wiley and Sons, Inc., New York, (1960).

4. R. K. Richards, "Digital Computer Components and Circuits" D. Van Nostrand Co., Inc., Princeton N. J. (1957).

5. "IRE Standards on Static Magnetic Storage: Definitions of Terms," *Proc IRE*. Vol. 47 No. 3, pp. 427-430 (March 1959).

6. H. J. Heijn and N. C. de Troye, "A Fast Method of Reading Magnetic Core Memories," *Philips Technical Review*, Vol 20, No. 7, pp. 193-207, (1958/59).

7. R. E. McMahon,"Survey of Memory Techniques Using Transistors" M.I.T. Linoln Lab., Lexinton Mass., Rept. 2G-24-82; (October 1, 1957).

8. J W. Forrester, "Digital Information Storage in Three Dimensions Using Magnetic Cores," *J. Appl. Phys.*, Vol. 22, pp. 44-48, (January 1951)

9. R. Straley, A. Hener, B Kane and G. Tkach, "A Miniature Memory Plane for Extreme Environmental Conditions." *J. App. Physics*, Supp. to Vol 31 No. 5, pp. 126-128 (May 1960).

10. G. H. Perry and S J Widdows, "Low Coercive-Force Ferrite Rings for a Fast Non-Distinctive Read Store," *Digest of Technical Papers* Internatl Solid State Circuits Conf. Phila., Pa , pp 58-59, (Feb 1960)

11 D. B. G Edwards, M. J Lanigan, and T Kilburn, "Ferrite-Core Memories with Rapid Cycle Times," *Proc IEE*, Vol. 107, Part B, No 36, pp. 305-598, (November 1960)

12 R. W. McKay, H. N Yu and C Pottle, "A One-Word Model of a Word Arrangement Memory," University of Illionis Graduate College Digital Computer Lab. Report No. 79, (May 1957).

13. J. A. Rajchman and A W. Lo, "The Transfluxor - A Magnetic Gate with Stored Variable Setting," *RCA Rev.*, Vol 16, pp. 303-311, (June 1955).

14. L P. Hunter and E. W Bauer, "High Speed Coincident Flux Storage Principles," *J. Appl. Phys.*, Vol. 27, pp 1257-1261, (November , 1956).

15. J. A. Baldwin, Jr and J L. Rogers, "Inhibited Flux—A New Mode of Operation of the Three-Hole Memory Core," *J. Appl. Phys.*, Suppl to Vol. 30, No. 4, pp 58S-59S, (April 1959).

16. H W. Abbott and J. J. Suran, "Multihole Ferrite Core Configurations and Applications," *Proc. IRE*, Vol. 45, pp. 1081-1093, (August, 1957)

17 H. D. Crane, "A High-Speed Logic System Using Magnetic-Elements and Connecting Wire Only," *PROC. IRE*, Vol 47, pp 63-73, (January, 1959).

18. C. L Wanlass and S D. Wanlass, "BIAX High Speed Magnetic Computer Element," *1959 IRE WESCON CONVENTION RECORD*, Part 4—Automatic Control: Electronic Computers; Information Theory, p. 40.

19. W Earl Stewart, *"Magnetic Recording Techniques,"* McGraw-Hill Book Co., Inc., (1958).

20 A. S. Hoagland and G. C. Bacon, "High-Density Digital Magnetic Recording Techniques," *PROC. IRE*, Vol 49, No 1, pp. 258-267, (January, 1961).

21. Eugene M Grabbe, Simon Ramo, and Dean E Wooldridge, *Handbook of Automation, Computation and Control*, Vol. 2, Chap 20, John Wiley and Sons, Inc , New York.

22. IBM Federal Systems Div., "High Speed Computational Techniques," Rome Air Dev. Center, Contract AF30(602)-2161.

REFERENCES

23. J. J. Raffel and D. O. Smith, "A Computer Memory Using Magnetic Films," UNESCO Natural Sciences Division, *International Conference on Information Processing*, Series K. 6 pp. 447-455.

24. S. Methfessel, W. E. Proebster and C. Kinberg, "Thin Magnetic Films," *International Data Processing Conference*, Paris (1959).

25. J. B. Goodenough and D. O. Smith, "The Magnetic Properties of Thin Films," Massachusetts Institute of Technology, PB 146498.

26. E. M. Bradley, "Making Reproducible Magnetic-Film Memories," *Electronics* pp. 78-81, (September 9, 1960).

27. Robert M. Tillman, "Fluxlok—A Nondestructive, Random-Access Electrically Alterable, High-Speed Memory Technique Using Standard Ferrite Memory Cores," *Trans. IRE PGEC* Vol. 9, No. 3, pp. 323-329, (September, 1960).

28. W. L. Shevel, Jr. and O. A. Gutwin, "Partial Switching, Nondestructive-Readout Storage System," *Digest of Technical Papers*, Solid State Circuits Conf. Phila. Pa. p. 62-63, (February, 1960).

29. Charles F. Pulvari, "Research on High Temperature Ferroelectric Storage Media," WADD Tr 60-146, (April, 1960).

30. J. R. Anderson, "Ferroelectric Devices," *Proceedings of the Solid State Devices Colloquium*, California Institute of Technology, (February 20-21, 1961).

31. H. Kallman and J. Rennert, "Research and Devleopment for the Study of the Storage of Electrical Energy with the Help of Persistent Internal Polarization in Phosphors," Army Contract DA 30-069-ORD-3075, Quarterly Progress Report No. 1, (October 1960).

32. Bureau of Standards, "A Diode-Capacitor Memory for High-Speed Electronic Computers," *Tech. News Bull. Nat. Bur. Stand.*, Vol. 37, pp. 171-173, (November, 1953).

33. T. Greenwood, "High Speed Barrier Grid Store," *Bell System Tech Journ.*, pp. 1195-1220, (September 1958).

34. M. S. Raphael and A. S. Robinson, "Digital Storage Using Neon Tubes," *Electronics*, Vol. 29, pp. 162-165, (July, 1956).

35. J. C. Miller, K. Li and A. W. Lo, "The Tunnel Diode as a Storage Element," *Digest of Technical Papers*, International Solid-State Circuits Conf. Phila., Pa., pp. 52-53, (February, 1960).

36. Ralph C. Johnston, "Considerations In The Design of A Random-Access Cryosar Memory," Report No. 53 G—0039,

37. R. C. A. "High-Speed Data Processor System Research Project Lightening," Interim Research Report No. 5A, Chapter 4, ASTIA No. AD246197.

38. D. Arenberg, "Basic Types of Delay Lines," *Arenberg Ultrasonic Lab, Inc.*, Instr. and Auto, p. 1676-1678, (October, 1958).

39. Harry H. Lockhart, "Recent Delay Line Applications," *Instruments and Automation*, Vo. 31, No. 10, (October, 1958).

40. J. R. Anderson, "Electrical Delay Lines for Digital Computer Applications," *Trans. IRE*, Vol. EC-2, pp. 5-13, (June, 1952).

41. H. Epstein and O. Stram, " Magnetostrictive Sonic Delay Line," *Rev. Sci. Instr.*, Vol 24, pp. 231-232, (March 1953).

42. C. G. Shook, "A digital Magnetic Wire Storage with Non-Destructive Read-Out," *IRE TRANS, PGE*, Vol. 10, pp. 56-62, (March 1961).

43. A. G. Anderson, R. L. Gorwin, E. L. Hahn, J. W. Horton, G. L. Tucker and R. M. Walker, "Spin Echo Serial Storage Memory," *J. App. Physics*, Vol. 26, No. 11, pp. 1324-1338, (November, 1955).

44. C. W. Hoover, G. Haugk and D. R. Herriott, "System Design of the Flying Spot Store," *Bell System Tech, J.* Vol. 38, No. 2, pp. 365-402, (March, 1959).

REFERENCES

45. G. W. King, (Director), "The Photoscopic Memory System," Final Report on Computer Set AN/GSQ-16(XW-1) Contract AF 30(602)-1823, ARDC.

46. Duncan H. Looney, "A Twistor Matrix Memory for Semipermanent Information," *Proc, WJCC*, pp. 36-40, (March, 1959).

47. H. R. Foglia, W. L. McDermid and H. E. Petersen, "Card Capacitor—A Semi-Permanent Read Only Memory," *IBM I. Res. and Dev.* Vol. 5, No. 1, pp. 67-68, (January, 1961).

48. T. Kilburn and R. L. Grinsdale,"A Digital Computer Store with Very Short Read time," *Proc IEE* Part B Vol. 107, No. 36, (November, 1960).

49. W. E. Glenn, "Thermoplastic Recording," *J. App. Physics*, Vol. 30, No. 12, p. 1870, (December, 1959).

50. E. K. Parker, "Research on High Density Large Capacity Thermoplastic Film Data Storage System," First Quarterly Report (1 Dec. 1959, 29 Feb. 1960), Proj. SCRAM.

51. General Electric, Mfg. Literature on Thermoplastic Recording Product Information Subsection Light Military Electronics Dept. Utica, New York.

52. D. A. Buck, "The Cryotron—A Superconductive Computer Component," *PROC IRE*, Vol. 44, pp. 482ƒ493, (April, 1956)

53. J. W. Crowe, "Trapped Flux Superconducting Memory," *IBM J. Res. and Dev.*, Vol. 1, pp. 294-303, (October, 1957).

54. J. W. Bremer, "Cryogenic Devices in Logical Circuitry and Storage," *Elec. Mfg.*, pp. 78-83, (February, 1958).

55. Robert R. Seeber, Jr., "Associative Self-Sorting Memory," *Proceedings of the EJCC*, pp. 179-188, (December 13-15, 1960).

56. V. L. Newhouse, et al, "End Fired Memory Uses Ferrite Plates," *Electronics*, 4 pp. (October 10, 1958).

57. J. A. Rajchman, "Ferrite Aperture Plate for Random Access Memory," *Proc EJCC*, pp. 107-115, (December, 1956).

58. K. Preston, Jr. and Q. W. Simkins, "Twistor Buffer Store, " *Digest of Tech. Papers, 1959 Solid-State Circuits Conf.*, Philadelphia, Pa, pp. 14-15, (February, 1959).

59. D. A. Meier, "Millimicrosecond Magnetic Switching and Storage Element," *J. Appl. Phys.*, Suppl to Vol. 30, 4 pp. 45S-46S; (April, 1959)

60. R. C. Minnick and R. L. Ashenhurst, "Multiple Coincidence Magnetic Storage Systems," *J. Appl. Phys.*, Vol. 26, pp. 575-579, (May, 1955).

61. H. P. Schleeppi, I. P. V. Carter,'Submicrosecond Core Memories Using Multiple Coincidence," *Trans. PGEC*-9, p. 192, (June 1960).

62. F. C. Williams, T. Kilburn, C. N. W. Litting, D. B. G. Edwards and G. R. Hoffman, "Recent Advances in Cathode-Ray Tube Storage," *Proc IEE*, Part II, Vol. 100, pp. 523-539, (October 1953) Discussion, pp. 540-543.

63. R. F. Fisher and P. Mallery, "Counter-Wrapped Twistor," *Proc. National Electronic Components Conference*, Wash. D.C. pp. 129-133, (May, 1960).

64 J. R. Anderson, "A New Type of Ferroelectric Shift Register," *Trans. PGEC*, Vol 5, pp. 184-191, (December, 1956).

65. C. F. Pulvari, "Ferroelectrics and Their Memory Applications," *Trans. IRE PGCP*, (March 1956).

66. M. Prutton, "Ferroelectrics and Computer Storage,'*Brit. IRE J.* pp. 93-99, (February, 1959).

67. S. Morleigh, "A Sensing System for Punched Cards or Continuous Punched Foil," *Electronic Engineering*, Vol. 31, M 373, pp. 140-141, (March 1959).

68. A. Kent and I. S. Isbell, "Soviet Documentation," *American Documentation*, Vol. 19 p. 13 (January 1959).

69. W. H. Kautz, "Constant-Weight Counters and Decoding Trees," *Trans. PGEC*, Vol 9, pp. 231-244, (June, 1960).

70. Electronic Design, "Large Parallel-Access, High Speed Disc File Cuts Storage Costs," Electronic Design, pp. 82-83, (March 1, 1961).

71. G. J. Axel, "Univac—Randex II Random Access Data Storage System," *Proc. of the EJCC*, pp. 189-203, (December 13-15, 1960).

72. "Technical Description of Telex Mass Memory Modules," Company Literature.

73. B. Widrow, "A Radio-Frequency Nondestructive Read-Out of Magnetic Core Memories," *IRE TRANS. ON ELECTRONIC COMPUTERS*, Vol. EC-3, pp. 12-15, (December, 1954).

74. E. Goto, "The Parametron, a Digital Computing Element Which Utilizes Parametric Oscillation," pp. 1304-1316, Proc IRE, (August, 1959).

75. Emery A. Coil, "A Multi Addressable Random Access File System," *1960 WESCON Convention Record*, Part 4, pp. 42-47, (August, 1960).

76. B. K. Green, "Chemical Switches," *Proceedings of An International Symposium on the Theory of Switching*, Harvard University, (2-5 April 1957).

77. Ludwig Mayer, "Magnetic Writing with an Electron Beam," *Journal of Applied Physics*, Vol 29, No. 10. pp. 1454-1456, (October, 1958).

IV RELATIONSHIP OF FUNDAMENTAL TECHNIQUES TO COMPLETED STORAGE UNITS

In the bit-storage-capacity *vs* read-access-time graph of Fig. 6, a large blank area clearly separates the storage units utilizing static access from those relying on dynamic access. We will refer to those on the left of this separation as *high-speed storage units* and those on the right as *back-up storage units*. Let us look at these groups individually and determine which of the techniques outlined in Sec. III contribute to the position on this graph and the cost of storage units. Also, let us examine briefly what techniques are likely to contribute to improvements in the near future.

A. HIGH SPEED STORAGE UNITS WITH STATIC ACCESS

1. General

It is interesting to note that, with very few exceptions, all of the storage units in this group use magnetic cores for the storage registers. These storage registers are of three types: the coincident-current single-core-per-bit, and the linear-select single-core and two-core-per-bit. A much more significant variation exists in the type of access equipment used to select and excite these storage registers. Most of these storage units with read/write cycle times in excess of 6 μsec make use of the two-dimensional coordinate switch[1] described in some detail in the technical supplement to this report. The most popular type of access with cycle times between 2 and 6 μsec makes use of transistor switches. Transistor switches are used in two basic modes: In the first, a driver switch is provided for each line of memory (or in some cases pairs of lines). In this mode of operation the switches are often several transistors in parallel in order to achieve the speed and power levels required. The "decoding" is done by diode[2] gates at the input to each switch. The other mode of transistor access is to provide a transistor decoding tree of relatively slow transistors to set up an access path; a single high-speed pulse driver (*i.e.*, 1 per dimension) then excites the desired storage register via this path.

Access techniques for storage units which take less than 2μsec[3,4,5,6] depend primarily upon the load-sharing zero-noise magnetic-core access switch. This switch is described in detail in the Technical Supplement to this report. In general, the switch permits no decoding, but does permit the use of a large number of drivers to sum their power into a single load, permitting the use of many low-power, high-speed drivers; *e.g.*, transistors. The input address must be recoded from the address given to the computer to the representative code state of the drivers necessary to excite the storage register corresponding to the input address. Since sufficient information is retained in these drivers to locate and stimulate the desired storage register, the input address may be changing prior to the completion of the read/write cycle, thus eliminating a part of the propagation-time loss by overlap.

The notable *exceptions* to magnetic-core storage within this group are the small, very high-speed, thin, magnetic-film storage units of Lincoln Labs,[7] TX-2 and the UNIVAC 1107; and the read-only stores like Bell Laboratories Flying Spot Store, Ferranti, Ltd Ferrite Rod Store[16] and IBM Capacitor Store.[17]

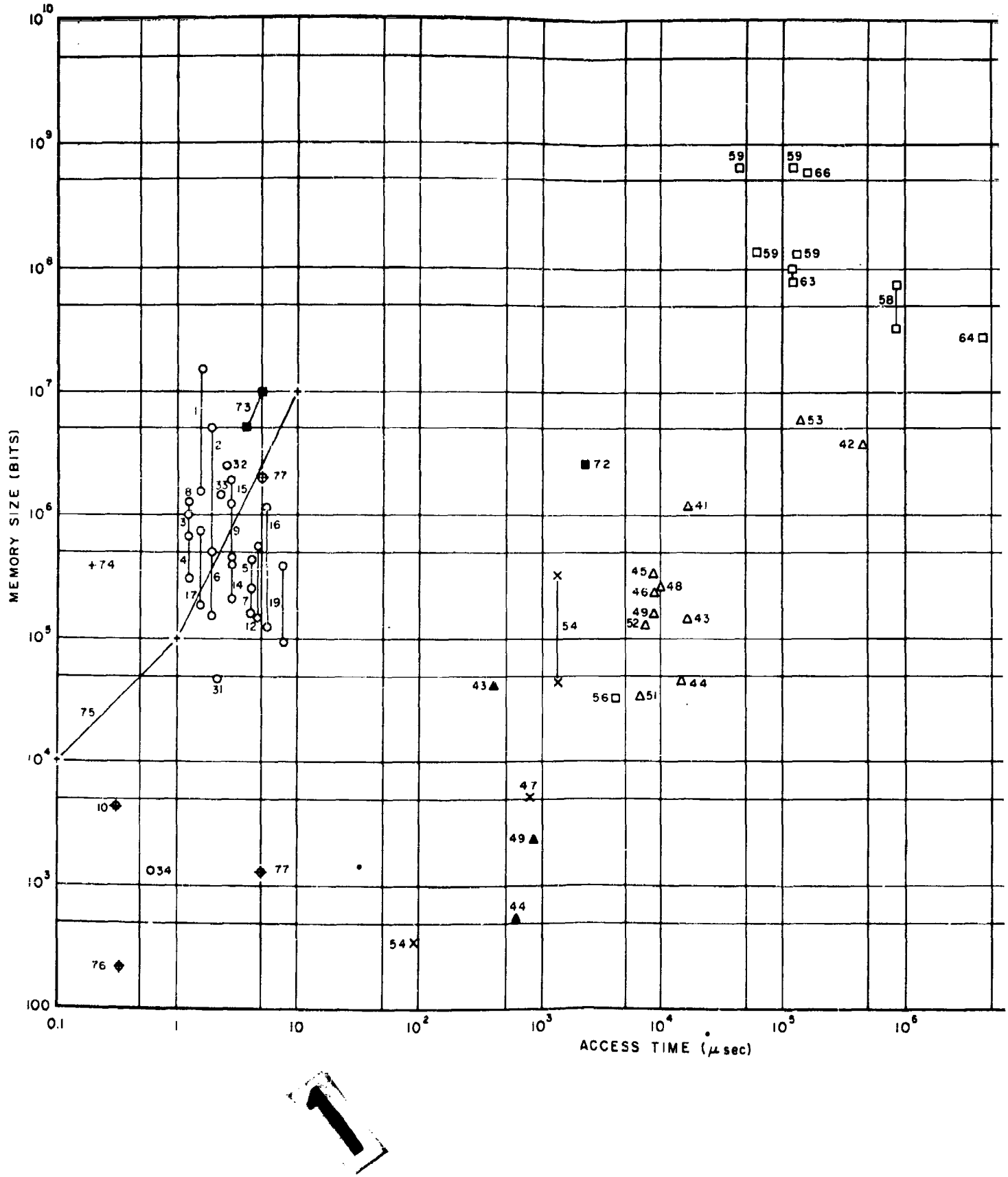
2. Capacity Considerations

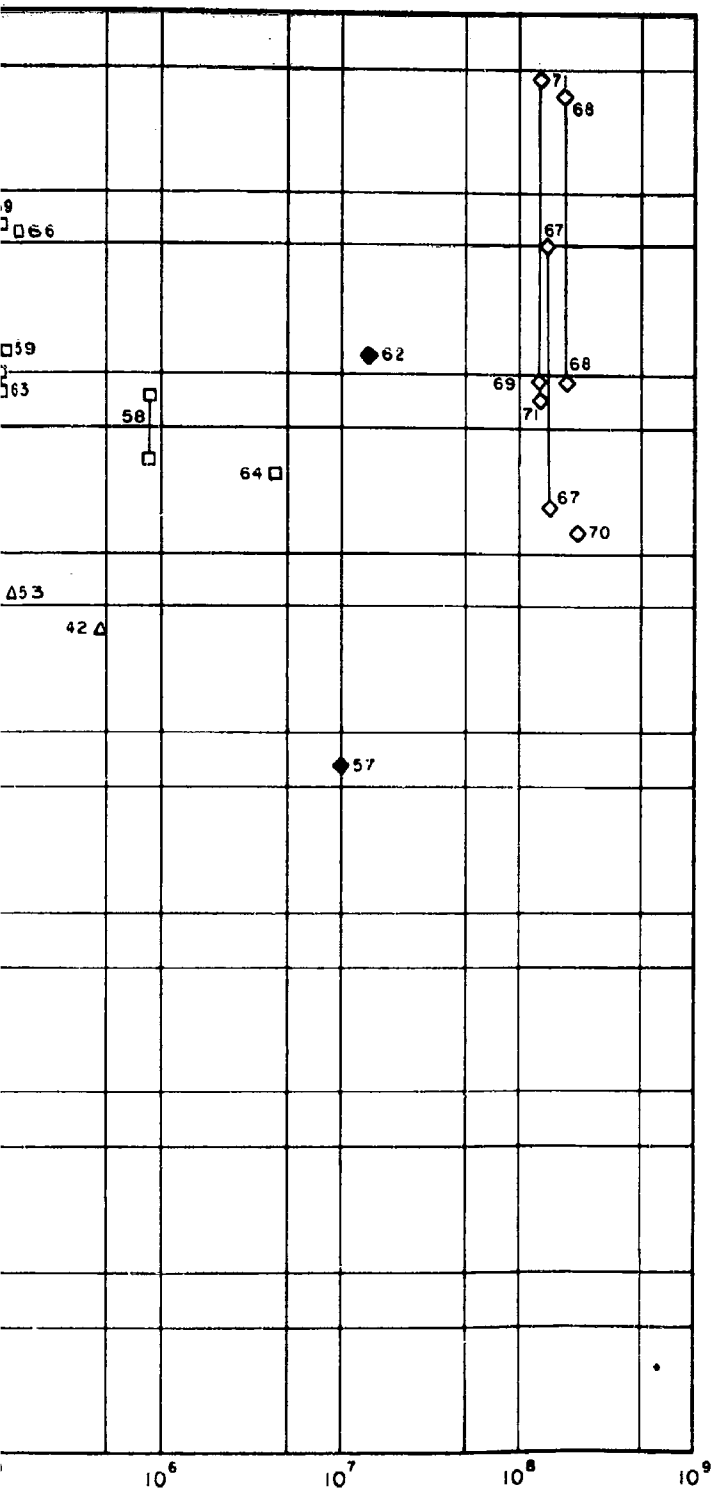
Three principal considerations limit the maximum storage capacity for any conceived unit: (1) the cost per bit to construct the storage unit; (2) the technique limitations, such as maximum number of storage cells a given access output is capable of exciting, or the problems due to excessive noise from partially disturbed cells[8,9] and (3) the ultimate reliability.

a. Cost per bit

For small-capacity storage units, say 10^4 bits and less, users can afford costs something like a dollar or more per bit. This will permit the use of very high-speed storage including circuit aggregates, such as flip flops and tunnel diodes which require the use of active elements. The advantage of the active elements is that access equipment need only carry signal power, since decoding stimulates the desired storage register without being required to supply the excitation *power*; hence very great speeds are possible.

Increased storage capacity to say 10^6 or 10^7 bits, generally demands techniques that are reduced in cost to a few tens of cents per


MEMORY SIZE (BITS)
ACCESS TIME (μsec)
10^10
10^9
10^8
10^7
10^6
10^5
10^4
10^3
100
0.1
1
10
10^2
10^3
10^4
10^5
10^6
59
59
66
59
59
63
58
64
53
42
72
41
45
46
48
49
52
43
54
56
51
44
43
47
49
44
54
10
34
77
76
75
74
1
73
2
32
77
33
15
8
3
9
16
4
6
5
14
17
7
19
12
31



LEGEND

- ○ MAGNETIC CORES
- ⊕ MAGNETIC THIN FILM
- △ MAGNETIC DRUM
- ▲ MAGNETIC DRUM HIGH SPEED REGISTER
- ■ PHOTOGRAPHIC
- □ MAGNETIC DISC
- ◇ MAGNETIC TAPE
- ◆ MAGNETIC TAPE STRIPS
- × MAGNETOSTRICTIVE DELAY LINE
- \+ MODULATED COUPLING

FIG. 6

CAPACITY VS. SPEED GRAPH
(Applicable to many existing storage units—the units shown by code numbers are identified in the Appendix)

bit, even if this requires giving up some speed. Magnetic core stores which use one or two cores per bit are in this range. They have been built with access times from one to 10 μsec, and access equipment generally based on the magnetic core. It appears technically feasible to increase the capacity of magnetic core storage units to something like 10^8 or 10^9. Such increases in size do not appear warranted at these prices and also put added strain on the necessity to wire discrete bits and adequate access equipment.

For storage units of greater than 10^8 it will almost certainly require the use of batch or continuous processes in order to reduce the cost per bit from the vicinity of a few cents, to fractions of a cent. Possible techniques for reducing costs are the twistor store, thin magnetic films, and the ferrite aperture plate.[10]

It is always possible to reduce the cost per bit by relaxing one or more of the requirements, such as relaxing the high-speed requirement in the host of dynamic access stores considered in Sec. D. Another possibility is to relax or eliminate the high-speed write requirement and maintain the high-speed random access only for reading. Examples of techniques of this type are the permanent magnet twistor store,[11] the ferrite rod[12] and the capacitor card store.[13] In the permanent magnet twistor store, the presence of a permanently magnetized spot on the card is detected by its biasing effect on the twistor element, which prevents switching in one mode and aids switching in another mode. The absence of such a spot permits the normal switching of the twistor. Such storage units, at present, are designed in the linear-select fashion (S_r approaching infinity), but this is to relax the square-loop requirements of the twistor rather than because of any fundamental need. The Kilburn rod used in the Atlas MUSE Computer must be designed linear-select with an infinite read-selection ratio. Ferrite rods are then placed in the vicinity of the intersection of the word and digit lines. The presence or absence of these rods modifies the coupling for a semipermanent store. A very ingenious device has been constructed for moving the rods rapidly in or out of position pneumatically. Writing is essentially serial access; as the machine travels, the track places rods in their correct position. Reading is random access, with an access time of approximately 0.2 μsec. The IBM capacitor card is likewise a linear-select arrangement in which the coupling between the intersection of word lines and digit lines is

modified by the presence or absence of a small capacitor. The cards are essentially punched paper cards of the standard IBM type with the exception that there is a metalized foil sandwiched into the card. The grounded foil forms a Faraday shield between selection lines and digit lines, preventing coupling at intersections. Where the shield is punched out, a capacitive coupling of approximately three picofarads is formed. These cards can be punched and handled on all standard punched-card handling equipment now in existence, and must then be inserted in a storage unit for use. Read times are random-access to linear-selected words, which may be either the columns or the rows of a card. The times can vary with the size of the storage unit, but are reported to be 0.1 μsec for stores of 10^4 bits, 1.0 μsec for 10^6 bits, and 10 μsec for 10^7 bits.

The second consideration in capacity is the technical feasibility of very large storage aggregates without the necessity of completely replicating the store. The two principal limiting factors are the maximum number of storage cells which a given access output is capable of exciting, and the accumulation of small noise sources that completely obliterate the signal. For instance, the accumulation of partial disturbs in coincident-current magnetic-core *unit* very rapidly increases beyond the output signal, and techniques such as checkerboarding and strobing of the output for optimum times have been developed to extend this range. The other limitation is the amount of high-speed drive available from a single access output. Increased speeds and increased capacity both mean increased back voltages and hence more power per access output. Load sharing and other redundancy techniques explained in the Technical Supplement to this report have shown that the addition of one set of redundant windings in a magnetic core access switch can double the power output.

The fact that in superconductive devices the resistance is *exactly* zero admits the possibility of eliminating the accumulation of a large number of minute noise sources. Thus cryogenics gives some hope of very large-capacity, random-access stores, particularly in the fixed or read-only modes.

The transition from small to very large-capacity static storage units puts an additional strain on component reliability. For instance, components that fail once in 10^8 hours are considered to be fairly reliable, *e.g.*, the inspected solder joint. However, in considering storage capacities of 10^8 or 10^9 bits, components of this order of reliability would mean

the storage unit would be failing on the average of several times per hour, even assuming only one such component per bit were required. Thus either super reliable components are required, or one or more of the following; distributed storage, redundancy in access, and error correcting codes must be used.

3. Speed Considerations

The limitations on speed of a particular static access storage unit can well be divided into three categories.[14] The first two categories have to do with the two parts of the read or write phase of the storage unit: (1) the reaction time of the storage register, and (2) the propagation and other miscellaneous times that complete the cycle time of the unit. The third category is the limitation in speed due to heating and power dissipation.

The reaction time for magnetic-core storage registers is generally the switching time of the cores themselves. The speed of switching is closely related to the magnitude of the exciting field by a relationship that is best described through the concept of a switching coefficient,[15,16] $S_w = T_s(H_s - H_o)$. That is, once the switching field, H_s, exceeds the threshold field, H_o, the switching time, T_s, is inversely proportional to the switching field. This coefficient remains essentially constant for a particular material, volume and path length of material, switching mode, and temperature. Present materials and sizes (magnetic cores of 80 mil OD × 50 mil ID, or 50 mil OD × 30 mil ID) have coefficients of approximately 1-2 oersted-microseconds for complete domain wall switching. Cores have recently been announced of materials which are 30 × 17 mils. and are still physically strong enough to permit handling. As the switching coefficient equation shows, it is possible to shorten the switching time by providing very high driving currents. However, in the coincident-current memory (indeed, in any storage unit of more than one read dimension) the read-selection ratio cannot generally exceed 2 without complex wiring, however, certain exceptions have been shown.[17,18] Under such practical limitations, switching typically takes approximately 1 μsec for the linear-select units. This can be reduced by overdrive to something approximating 0.2 μsec for read, but the write time remains the same. There are a number of ways of reducing this reaction time, one of which is to physically reduce the size of the core. Another is to electrically reduce the size of the core

by means of partial switching.[19,20,21] Partial switching typically overdrives in the read or reset direction so that one remanent state is on a major loop but carefully controls the pulse width and amplitude in the write direction to switch only a given percentage of the flux available in the core. Impulse switching offers another opportunity of controlling the partial switching.[21]

Another very powerful means of increasing the speed or decreasing the reaction time of the storage cells is through rotational switching of the magnetic domains as opposed to domain wall motion. This is principally exploited in thin magnetic films, but has also been demonstrated in cores by the Fluxlok technique[22] and in the strong overdrive techniques.[19] These rotational switching modes are limited in their reaction time only by the rise time of the excitation field. Thus in any storage unit in which the storage registers exploit rotational switching, the time required to complete a read or write cycle is almost completely dependent upon the access equipment and is, therefore, almost completely independent of the storage mechanism. This again points out the tremendous need for detailed studies of access techniques.

The second major division of the time to complete the read or write phase of the storage unit is the propagation time and the miscellaneous time losses. These may include switching times involved in the input address register, propagation time through decoders, drivers and access switches, the physical propagation time due to size alone from access equipment to register, delay time in strobing and sensing, and the propagation time from sensing equipment to input/output register. Physical size alone becomes important in very high-speed storage units, when it is realized that signal information travels only 8 to 10 inches per nanosecond, depending upon the material. Hence for a 10 nanosecond cycle time (assuming no delays in reaction time of the storage register), the entire distance from the input/output to the farthest storage register could only be a few feet. There are opportunities for a certain amount of overlap with magnetic-core access switches, particularly of the load-sharing type. For instance, the access switch drivers maintain all the necessary information to specify the address; hence, once the signal has propagated through the recoders to the access drivers, the information in the address register is no longer needed and may begin changing before the end of the cycle involved. Overlap procedures of this type require very careful design.

An important limit to the speed of operation is the temperature rise, either locally or generally within the storage unit.[4] Coincident-current memories in particular require very high uniformity in core-to-core properties. Thus, local differences in temperatures, whether due to repeated addressing of nearby registers or due to unequal cooling, can cause malfunction of the storage unit. Increased packing densities required for reducing propagation times tend to dissipate larger amounts of energy per unit volume.

B. DYNAMIC ACCESS STORAGE UNITS

1. General

The one feature which all storage units on the right of Fig. 6 have in common is that dynamic motion is involved in the access. There are a wide variety of techniques represented. The most prevalent storage units in this group are designed around magnetic drums or magnetostrictive delay lines, if under approximately 10^7 bits capacity, and around magnetic discs or tape strips if over this capacity. All of these employ cyclic access, thus reducing the amount of read/write circuitry per unit storage capacity far below that of static connections. Larger-capacity, slower-speed units of this group naturally overlap with external storage or input/output units which are not included but would fall in the upper right-hand portion of the graph in Fig. 6. Such units are generally typified by dynamic serial access as in magnetic tape, punched paper tape, and punched cards.

Let us define a *group* of storage cells as being the total number of cells which connect with a single read/write channel during a single cycle of access. This may be one or many words (storage registers). Then the connection between each such group and the input/output terminals of the storage unit are subject to the same descriptive terms as the connections between access and storage registers. That is, a storage unit may be cyclic but have separate read/write circuitry for each *group*. Therefore, each group would be directly wired or statically accessed even though the storage unit is essentially cyclic. This is necessary, for instance, in the case of delay lines where the read/write circuitry must be provided for each group (individual delay line) for regeneration of the stored data. Also, this is generally true for magnetic drums. In this case the use of high-speed circulating registers on a small percentage of the groups is one technique for reducing the average read access time by the ratio of the number of such registers per group.

Alternatively, a single read/write channel may be provided which has a dynamic, serial connection with the groups, e.g., the Remington-Rand flying-head drums.[2] Here, a single head is moved along the drum (parallel to its axis) from one track to the next in a serial, reversible fashion. The ratio of the number of read/write channels to the number of storage cells is important in determining the total cost and speed of a storage unit. Early disc storage units had only one read/write channel, this head could move linearly in two dimensions but not simultaneously. Speed increases have been made by including multiple heads per arm with one arm for each disc face. This greatly reduces the mechanical distance that heads must travel, and hence reduces the access time to a group. Also by simultaneously positioning the arms on each surface, parallel read-out of individual words is accomplished. Present storage units of this type permit transfer rates of 6 μsec per word with up to 48 bits per word.[2]

Further speed increases are possible in several ways. Present recording densities on the surface are quite conservative, generally only a few hundred bits per inch. Such densities will increase with further development. Improved positioning mechanisms will reduce the access time due to positioning (at present the major time delay). Also it will permit smaller rotating parts and higher rotating speeds which in turn reduces the cyclic access time. Cyclic access times can also be reduced by including more access equipment per recording surface, but at greatly increased cost per bit.

2. Large Capacity Nonmagnetic Storage Units

Although the area of very large capacity stores is at present dominated by magnetic surface recording, this position is being challenged by several schemes.

The flying-spot store[24] was developed at Bell Laboratories. This storage unit uses photographic plates for the data storage and a flying-spot-scanner, photo-multiplier for access and sensing. The unit is operated in the addressable mode. It is essentially a fixed but changeable store with pseudo-random access. The number of bits per word determines the required number of plates, and the number of bits per plate determines the number of registers in the storage unit. A separate optical system is used with each plate, so that the image of the CRT face is individually focused on each plate. Also each plate has a separate photo multiplier. Access to

a particular register is made by positioning the electron beam inside the CRT. The phosphor screen converts the electron-beam to a light beam which is focused on each bit plate simultaneously for parallel read-out. At present, systems have been demonstrated which store 131,000 76-bit words with 5 μsec read-access time and 65,000 76-bit words with 4 μsec read-access time. A limiting feature of the maximum capacity is the number of suitable spots that can be generated on the CRT face. The accurate positioning of these spots now requires a servo system.

The photoscopic store, developed at IBM for the AN/GSQ-16 language translator,[25] also employs photographic storage and a flying spot scanner for access. The data are not stored on stationary plates, but on a single annulus of a revolving glass plate. Hence, the unit is cyclicly accessed. The CRT and a movable lens are used essentially radially for track selection, and a servo loop is used to position the light beam accurately. As presently demonstrated, the unit stores 21×10^6 bits, with an average read-access time of 25 milliseconds, but may soon be increased to 31×10^6 bits.

A storage unit is being developed at General Electric which employs thermoplastic plates for storage and a flying spot scanner for access.[26] Unlike the Bell Labs flying spot store, the light beam from the CRT face is directed at only one plate at a time and the bits are read out in serial by scanning the beam. The principal advantage of the thermoplastic storage is that it is erasable under control of the parent system. The unit is presently planned to store 38×10^7 bits with a maximum access time of 1 millisecond.

Another interesting approach is being pursued by MIT and the Hydel Corp. The storage is on stationary photographic plates which are illuminated. The image of these plates is swept past a set of photo multipliers by an N-sided rotating mirror. Such a storage unit would be fixed and cyclic. While an experimental model is capable of storing over 10^7 bit, an average access time is not known.

A very interesting proposed scheme makes use of the basic electron-beam-activated machining process.[27] In general, the storage method consists of machining ordered structures in thin films deposited on a movable substrate, using a fixed-position, electro-statically operated electron-optical system. The same electron-optical system operating in a different mode is used to read out stored information electronically. Well-developed

techniques of modern electron-microscopy are available, including high resolution and high rates of processing and read-out. All processes will be conducted in ultra-high vacuum, a required condition if long-term stability of stored information and the electron-optical system is to be maintained.

C. FIGURE OF MERIT

It is rather difficult to offer a "figure of merit" which covers all types of storage units and is of any real value. Each type of storage unit must fit its particular task and be as economical as possible. However, if a line is drawn on Fig. 6 connecting the leftmost units having dynamic access, it is seen to have a slope of approximately 2. Thus if each unit along this line is to have an equal figure of merit, this would yield

$$\text{FM} = \log_{10}(\text{bit capacity}) - 2\log_{10}(\text{access time})$$

$$= \log_{10}\left(\frac{C}{t^2}\right) \quad .$$

In order to use non-negative figures of merit, the capacity should be in bits and the read-access time in seconds. The inclusion of the access time in the denominator raised to the second power leads to the prediction that capacity can be increased by two orders of magnitude while only suffering one order loss in speed.

REFERENCES

1. J. A. Rajchman "Static Magnetic Matrix Memory and Switching Circuits" *RCA Rev.*, Vol. 13, pp. 183-201; (June, 1952).

2. R. E. McMahon and F. L. McNamara "Transistor Core Memory," M.I.T. Lincoln Lab., Lexington, Mass., Tech. Rept. No. 133; (November 13, 1956)

3. G. Constantine, Jr., "A Load-Sharing Matrix Switch," *IBM J. Res. and Dev.*; pp. 204-211 (July, 1958)

4. M. P. Marcus, (IBM) "Doubling the Efficiency of the Load-Sharing Matrix Switch," *IBM J. Res. and Dev.*, Vol. 3, No. 2, pp. 195-196 (1959).

5. G. Constantine, Jr., "New Developments in Load-Sharing Matrix Switches," *IBM J. Res. and Dev.*, Vol. 4, No. 4, pp. 418-422, (October 1960).

6. R. T. Chien, "A Class of Optimal Noiseless Load-Sharing Matrix Switches," *IBM J. Res. and Dev.*, Vol. 4, No. 4, pp. 414-417, (October 1960).

7. J. J. Raffel and D. O. Smith, "A Computer Memory Using Magnetic Films," UNESCO Natural Sciences Division, *International Conference on Information Processing*, Series K.6 pp. 447-455 (June 1959)

8. J. D. Childress, "The Noise Problem in the Coincident Current Memory Matrix," M.I.T. Lincoln Lab., Lexington, Mass., Div. 6, 6M-4153: (Bebruary 13, 1956).

9. McNamara, "The Noise Problem in a Coincident-Current Core Memory," *Trans. IRE PGI*, Vol. 1-6, pp. 153-156, (June 1957).

10. D. H. Looney, "Recent Advances in Magnetic Devices for Computers," *J. Appl. Physics*, Suppl. to Vol. 30.4, pp. 45S-46S; (April, 1959)

11. Duncan H. Looney "A Twistor Matrix Memory for Semipermanent Information," *Proc. WJCC*, pp. 36-40; (March 1959).

12. T. Kilburn and R. L. Grinsdale, "A Digital Computer Store with Very Short Read Time," *Proc. IEE* Part B Vol. 107 No. 36 (November 1960).

13. H. R. Foglia, W. L. McDermid, and H. E. Petersen, "Card Capacitor - A Semi-Permanent Read Only Memory," *IBM J. Res. and Dev.*, Vol. 5, No. 1, pp. 67-68 (January 1961).

14. B. T. Goda, W. R. Johnston, S. Markowitz, M. Rosenberg, and R. Stuart-Williams, "All-Transistor Magnetic-Core Memories," *AIEE Transactions*, Part I (Communications and Electronics), Vol. 78, pp. 666-672; (November 1959).

15. A. J. Meyerhoff, *Digital Magnetic Circuits*, John Wiley and Sons, Inc., New York, (1960).

16. N. Menyuk and J. G. Goodenough, "Magnetic Materials for Digital Computer Components. I. A Theory of Flux Reversal in Polycrystalline Ferromagnetics," *J. Appl. Phys.*, Vol. 26, pp. 8-18 (January 1955).

17. R. L. Ashenhurst, "The Structure of Multiple-Coincidence Selection Systems," Doctorate Thesis, Div. of Eng. and Applied Physics, Harvard University, (May 1956).

18. H. P. Schlaeppi, I. P. V. Carter, "Submicrosecond Core Memories Using Multiple Coincidence," Trans PGEC-9 p. 192 (June 1960).

19. G. H. Perry and S. J. Widdows, "Low Coercive-Force Ferrite Rings for a Fast Non-Distinctive Read Store," *Digest of Technical Papers*, Internatl. Solid State Circuits Conf. Phila., Pa., pp. 58-59 (February 1960).

20. W. L. Shevel, Jr. and O. A. Gertwin, "Partial Switching, Nondestructive-Readout Storage System," *Digest of Technical Papers*, Solid State Circuits Conf., Phila., Pa., pp. 62-63, (February 1960).

21. Roger H. Tancrell and Robert E. McMahon, "Studies in Partial Switching of Ferrite Cores," *J. Appl. Phys.*, Vol. 31, No. 5 pp. 762-771 (May 1960).

REFERENCES

22. G. J. Axel, "Univac-Randex II Random Access Data Storage System," *Proc. EJCC*, pp. 189-203 (December 13-15, 1960).

23. Electronic Design "Large Parallel-Access, High Speed Disc File Cuts Storage Costs," Electronic Design pp. 82-83 (March 1, 1961).

24. C. W. Hover, G. Haugk and D. R. Herriott, "System Design of the Flying Spot Store," *Bell System Tech. J.*, Vol. 38, No. 2, pp. 365-402 (March 1959).

25. G. W. King, "The Photoscopic Memory System," Final Report on Computor Set AN/GSQ-16(XW-1) Contract AF 30(602)-1823 ARDC

26. E. K. Parker, "Research on High Density Large Capacity Thermoplastic Film Data Storage System," Quar. Prog. Rept. 2, Proj. SCRAM. (Contract DA 36-039-sc-85118, Proj. 3A-99-22-001-04) General Electric Co., Schenectady, N.Y. (1 March - 31 May 1960).

27. K. R. Shoulders, "Research and Micro-Electronics Using Electron-Beam-Activated Machining Techniques." Contract Nonr-2887(00) Office of Naval Research, Washington, D. C.

V SUMMARY AND CONCLUSIONS

We have used the artifice of a conceptual model of a storage unit in order to classify the various kinds of storage units according to their terminal characteristics. The important terminal characteristics are the storage capacity, speed and order of access, the operating mode, and the permanence of the stored data. We dissected this model into four fundamental parts, an aggregate of storage registers, access equipment for selection and excitation of the desired register, the sensing equipment for determining the data stored in the register, and the organizational scheme used for interconnection. The various techniques for achieving these fundamental operations are outlined and discussed. The relation between the use of particular techniques in a storage unit and the position of that storage unit on the capacity *vs* speed graph is shown with some predictions for improvements.

Before very large capacity, fast-storage units of perhaps one billion bits with only a few microseconds access time can become possible, this survey shows that improved methods of static access are required. Because this conclusion came early in the project, static random-access techniques were given special attention. Indeed, a mathematical model which permits the inclusion of many known magnetic-core access switches was developed. More important, an algorithmic procedure for the design of the most economical, reliable switch available for any given set of requirements imposed by available drivers and current driven storage registers is developed. This special study and development is printed separately (RADC-TR-61-117B) and titled Magnetic Core Access Switches, Technical Supplement to RADC-TR-61-117A. For convenience, the summary and conclusions section of that report are repeated here.

V SUMMARY AND CONCLUSIONS OF TECHNICAL SUPPLEMENT

A. SUMMARY

The results of the report may be summarized briefly in two categories:

(1) *Systematic Study of Conventional Magnetic Core Access Switches*--The conventional coordinate access switches of Olsen, Rajchman, and others were used as a basis on which a general mathematical model for the coordinate access switch was established. Similarly, a model was developed which generalized the load-sharing zero-noise switches of Constantine, Marcus, and Chien.

(2) *Development of New and Promising Magnetic Core Access Switches*—It was found that certain specializations of the general mathematical model led to many novel switches. Examples of these new switches are load-sharing coordinate switches which have more outputs than inputs, and load-sharing zero-noise switches for which the designer is allowed more freedom in choosing the load-sharing factor. Algorithms and tables have been developed to aid the designer in finding the appropriate switch for his application.

For a more detailed summary, in *Section I* magnetic core access switches were defined, and their use in storage systems was shown. In *Section II*, a coordinate square switch was described in terms of three matrices: a winding matrix which indicated the wiring pattern, a selection matrix which contained all allowable ways of energizing the drivers, and an excitation matrix which gave the magnetomotive forces on the cores for all allowable ways of energizing the drivers. It was shown in this section that the matrices had better properties if the description of the bias winding was kept separate. Such pseudo switches were termed basic switches, and the addition of the bias was considered as an augmentation. Several other augmentations were considered: negative windings, non-unit windings, inhibiting drivers, and redundant windings. The negative winding and inhibiting driver augmentations were shown individually to be equivalent to the bias augmentation. The non-unit winding augmentation allows flexibility in choosing appropriate operating voltages and currents. The redundant winding augmentation is an original contribution of this report;

it allows the designer to obtain a pulse power on the selected output line greater than the input power delivered by any one driver.

The coordinate switch was further generalized to include non-square switches. All of the augmentations were combined into a general non-square switch, and the properties of this switch were discussed in some detail. It was shown that a number of access switches which have been described in the literature correspond to special cases of the generalized non-square switch; in addition the model yields a wide range of access switches which have not previously been published.

An additional subject which was treated in Sec. II and in the Appendices is that of design algorithms and aids for evaluating alternative switches. In particular, techniques were developed for producing the various matrices which describe the construction and operation of coordinate access switches. Wherever practicable these techniques were reduced to the simplest terms, such that the designer may write out the required matrices by making appropriate references to the design tables which are included in Sec. II and the appendices.

Section II concluded with the development of a cost model for coordinate switches. Given the unit cost of the components which make up a switch, the model allows choice of the least expensive switch. The model is useful in a number of other ways; for example, it allows the choice of the most reliable of a group of designs.

In *Section III* methods were developed for improving upon the coordinate switch by reducing the numbers of drivers or windings, or both. Some of these methods involved winding organizations different from the coordinate switch; others involved the introduction of diodes to route the driver outputs. An example of a switch using output logic was discussed and developed into a universal recoder.

Section IV contains a review of the current knowledge of a recent and important class of access switches, known as load-sharing zero-noise switches. These switches were compared, and a theorem was proven that these switches may have no more outputs than inputs. Some new classes of zero-noise switches were developed from load-sharing coordinate switches. These new switches allow achievement of larger numbers of outputs than was practical with conventional load sharing switches. Furthermore, all the known switches and certain of the new switches were

shown to be special cases of a more general class of zero-noise load-sharing switches that are based on balanced incomplete block theory. Finally techniques were developed for combining given switch designs into still more designs by using switch matrices as the elements of a switch matrix The resulting techniques allow the designer of zero noise load sharing switches far greater freedom than was formerly available.

B. CONCLUSIONS

1. Other Areas of Application for the Results

While the consideration in this report has been the systematic study and logical design of magnetic core access switches, it should be clear that other devices might be used in place of the magnetic cores with only minor alterations in the techniques which have been described. It was mentioned in the report in several connections that magnetic core access switches correspond to a special case of linear-input logic; consequently, other devices capable of performing this type logic are potentially suitable for alternative access switches. Possible examples are Kirchhoff resistor-adders, parametrons, certain multiapertured magnetic devices, multiple-coil relays, and others

It should be noted also that very few assumptions were made in this report on the nature of the storage devices themselves; although individual rectangular-loop magnetic cores organized in a coincident-current array were tacitly assumed The results of this report are essentially unchanged if for instance, a linear-select organization is used for the storage cores, and indeed if other devices are used in place of the storage cores Examples of such alternative devices might be magnetic aperture plates, tunnel diode storage arrays, and electroluminescent-photoconductive arrays . Similarly, the nature of the signal which is delivered by the access switch to the storage may vary from the pulse pair assumed in this report without essential changes in the results. For instance, very short or otherwise especially-shaped pulses may be called for in order to operate in various ways, such as in the partial-switching mode. On the other hand, the access switch may be called upon to deliver a sinusoidal signal on the selected output line, or perhaps to vary the phase of the signal on the selected line. These requirements would be appropriate to certain frequency-access methods. For such situations, some of the details of the techniques covered in this report would change, but the bulk of the results would remain.

While the access switches described in this report relate to random-access storage systems which may be altered electrically, there is nothing to keep the results from being used for other forms of storage systems. For instance, the access switches of this report may be used in connection with read-only storage systems; indeed, such systems involve little more than the access switch. Similarly, access switches may be considered as a special type of multiple-output network; and as such they may be used in applications having little to do with storage. For instance, it is not too difficult to conceive of a class of interesting pulse distributors based on the load-sharing access switches which have been discussed.

2. Suggestions for Further Work

While magnetic core access switches have been studied in some detail in this report, it appears that considerable work remains to be done. Such problems as the design of the drivers and of the signal recoders need to be considered, and the many new access switches disclosed in this report need to be evaluated by appropriate experimental work. While a general model for coordinate switches was developed in the report such that any switch of this class may be constructed by the application of the tabular techniques which were described, the load-sharing zero-noise switches do not easily fit this model. In fact, it is not yet certain that the most general class of such switches has been discovered. As a next step in this work, it would seem very desirable to develop even more general models than have been displayed in this report, with the hope of obtaining even more new access switches and of further increasing the degree of flexibility afforded the designer in his choice of the proper access switch for any particular application.

APPENDIX

The following is the list of storage units whose capacity and speed are plotted in Figure 6. The first column lists the code numbers of that figure. Column two lists the manufacturer and computer of which the storage unit is a part or the model number of the storage unit itself. Column three lists the storage capacity in thousands of registers or words. Column four is the number of digits (*b* = binary, *d* = decimal, *a* = alphanumeric) per word or register. Column five then translates these two into bit capacity of the storage unit. Column six lists the average read access time where known. Column seven is the read/write cycle time. In Figure 6 if read access time was not known separately, one half the R/W cycle time was used. Column eight lists the transfer rates of several back-up storage units in thousands of characters per second.

APPENDIX

NUMBER	MANUFACTURER AND COMPUTER TYPE	NUMBER OF STORAGE REGISTERS (thousands)	DIGITS PER REGISTER	BIT CAPACITY (thousands)	READ ACCESS TIME AVERAGE (μs)	R/W CYCLE TIME (μs)	CHARACTER TRANSFER RATE (thousands/sec)
1	IBM 7030 Stretch	16	64b	1,024	1.6	2.0	
				16,768	1.6	2.0	
2	UNIVAC LARC	10	12d	500	2	4	
		97	12d	5,000	2	4	
3	IBM 7090	32	36b	1,052		2.2	
4	IBM 7080	60	1a	320		2.2	
		80	1a	640		2.2	
		1	1a	4		1.1	
5	UNIVAC 1105	8	36b	288		8	
		12	36b	432		8	
6	IBM 709 Uses 738	4	36b	144	4	12	
	Mag. Core Mem.	32	36b	1,296	4	12	
7	UNIVAC 1103A	4	36b	144		8	
		12	36b	432		8	
8	CONTROL DATA	6.4	48b	384		2.2	
		6.4	48b	1,536		2.2	
9	RCA 601	8	56b	448		0.9	
	Mag. Mem. No. 661	32	56b	1,792		1.5	
10	UNIVAC 1107 Thin Film	0.128	32b	4.6	0.3	0.6	
11	PHILCO 2000	4	48b	192	5 and 1	10 and 2	
	220^{-4} Memory	32		1,536			
12	IBM 705	20	1a	140	5	9	
	Mag. Mem. No. 739	80	1a	560	5	9	
		40	1a	280	5	9	
13	UNIVAC II	2	12a	144		40	
14	IBM 7070	5	10d	200		6	
	Mag. Mem. No. 7301-1	5	10d	200		6	
	Mag. Mem. No. 7301-2	10		400		6	
	Mag. Mem. No. 7301-3 (high speed)	5		200		4	
	Mag. Mem. No. 7301-4 (high speed)	10		400		4	
14 1	IBM 7074	5	10d	200		4	
15	Honeywell H-800	4	12d	192		6	
		32	12d	1,536		6	
16	Bendix G-20	4	32b	128	5.6	6	
		32	32b	1,024	5.6	6	
17	UNIVAC III	3	6d	192	1.7	4.5	
		32	6d	768	1.7	4.5	
18	Burroughs 220	2		80	5	10	
	Mem. Type 381-2	5		200	5	10	
		10		400	5	10	
19	RCA 501	16.3	1a	98	7.5	15	
	Type 561-1	16.3			7.5	15	
	Type 561-2	32.7			7.5	15	
	Type 561-3	49.1			7.5	15	
	Type 561-4	65.5		393	7.5	15	

NUMBER	MANUFACTURER AND COMPUTER TYPE	NUMBER OF STORAGE REGISTERS (thousands)	DIGITS PER REGISTER	BIT CAPACITY (thousands)	READ ACCESS TIME AVERAGE (μs)	R/W CYCLE TIME (μs)	CHARACTER TRANSFER RATE (thousands/sec)
20	GE 210	4 8	6d 6d	96 192		32 32	
21	NCR 304	2 4	10a	120 240		60 60	
22	UNIVAC File I	0.020	12a	1.54		900	
23	IBM 650	0.060	10d	2.5		100	
24	Honeywell H-400	1 4	12d	48 192		8 8	
25	GE 225	2 16	21b	40 320		20 20	
26	IBM 1401 Core Unit 1406-1 1406-2 1406-3	1.4-16 4 8 12	1a	8.4-12.8 24 48 72		11.5	
27	RCA 301	10 20	1a	60 120		7 7	
28	DEC PDP-3	4 32	36b 36b	144 1,052		5 5	
29	DEC PDP-1	1 4	18b	18 72		5 5	
30	IBM 1620 1623-1 1623-2	20 20 40	1d 1d 1d	80 80 160		20	
31	Control Date 160	4	12b	49	2.2	6.4	
32	MIT-Lincoln Labs TX-2 "S" Mem.			2,500	2.8	6.5	
33	MIT Lincoln Labs TX-2 "T" Mem.			151	2.4	5.5	
34	MIT-Lincoln Labs TX-2 "X" Mem.	64 wds	19b	1.2	0.6	4	
35	Sylvania Mobidic	4 28	38b 38b	160		8	
36	Telemeter Mag. RB	0.256-1	4-206	20.5	5	10	
37	Telemeter Mag. LQ	8	2-80b	656 max	0.9	1.5	
38	TM 144-BQ8			1.2	7		
40	NCR 315	10 20 40	12b	120 240 480		6 6 6	
	NCR 316-3 Memory	10	12b	120		6	
41	UNIVAC File I Model "C" Drum	180	1a	1,080	17,000		
42	UNIVAC File I Randex Drum (2 drums)	6,000	1a	36,000	400,000		

APPENDIX *Continued*

NUMBER	MANUFACTURER AND COMPUTER TYPE	NUMBER OF STORAGE REGISTERS (thousands)	DIGITS PER REGISTER	BIT CAPACITY (thousands)	READ ACCESS TIME AVERAGE (μs)	R/W CYCLE TIME (μs)	CHARACTER TRANSFER RATE (thousands/sec)
43	UNIVAC Solid State 80/90 Drum	4 1	10d 10d	160 40	1,700 425		
44	BENDIX G-15 Drum	2 0.016	29 29	58 0.5	14,500 540		
45	GE 225 Drum (Auxiliary)			343	8,300		
46	RPC-4000 Drum	8	32	256	8,500		
47	RPC-9000 Magneto Striction	72	12a	5.2	800		
48	ALWAC-III-E Drum EL-Tronics	8	33b	260	9,000		
49	ElectroData 205 Drum	4 0.8	10d 10d	160 2.4	8,500 850		
50	Monorobot IX	0.152	1d	1			
51	Monorobot XI Drum	1	32b	32	6,000		
52	LPG-30 Royal McBee Drum	4	31b	124	7,500		
53	RCA 501 567 Drum File	1,500	1d	6,000	190,000		
54	Packard Bell PB-250 Magnetostrictive delay	16 16	22b 22b	0.352 0.352	90 1,500		
55	IBM 705 734 Mag. Drum	60	1a	360	8,000		
56	LFE Bernoulli Disc			32.7	4,000		
57	Shepherd TD-100 Bin tape deck			640	10 sec		
58	IBM RAMAC 7300-1 Disc Storage 7300-2 Disc Storage	6,000 12,000	1d 1a	36,000 72,000	< 1 sec < 1 sec		
59	Telex Disc File Telex I Telex IA Telex II Telex IIA			154,000 154,000 617,000 617,000	158,000 53,000 125,000 42,000		
60	Datamatic 1000 Magnetic file tape	37,200	1d	186,800			
61	NCR 304 330 Mag. Tape Handler (deck)			75,000			
62	ElectroData Data File Mod. 560	22,000	1d	110,000	14 sec		

NUMBER	MANUFACTURER AND COMPUTER TYPE	NUMBER OF STORAGE REGISTERS (thousands)	DIGITS PER REGISTER	BIT CAPACITY (thousands)	READ ACCESS TIME AVERAGE (μs)	R/W CYCLE TIME (μs)	CHARACTER TRANSFER RATE (thousands/sec)
63	GE Disc File Mass Random Access Memory	 75,000 100,000	 1a 1a	 	 150,000 150,000	 	
64	RCA 301 361 Record File	4,600	1a	27,600	4.25 sec		
65	RPC-9000 - Tape Loops	1,000	1a	7,000			
66	Bryant-4000 Mag. Disc File			720,000	167,000		160 (bit or word)
67	Remington Rand UNIVAC II Uniservo Tape 16 tape decks			37,000 592,000	140 sec 140 sec		25 25
68	IBM 729 II 40 tape decks			98,000 3.9×10^6	 140 sec		41 41
69	IBM 729 IV 40 tape decks			98,000 3.9×10^6	130 sec 130 sec		60 60
70	IBM 727 III Tape deck			14,000	180 sec		15
71	RCA 581 63			75,000 4.5×10^6	1.4 sec 1.4 sec		15 15
72	IBM AN/GSQ-16 Photoscopic Store			30,000	25,000		
73	Bell Laboratories Flying Spot Store	131,000 65,500	76b 76b	10,000 5,000	5 4		
74	Ferranti, Ltd. Ferrite Rod	8,000	50b	400	0.2		
75	IBM Card Capacitor	10 0.1 0.001	960/card 960/card 960/card	10,000 100 10	10 1 0.1		
76	Lincoln Labs Configuration Control Thin film store	0.032	10b	0.320	0.4		
77	Bell Laboratories Twistor Store	512	26b	13,312	5		

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